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ADDENDUM

Pocket of inside rear cover.

MODEL FPP-100 FOUR POINT PROBE

SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION. The FPP-100 was designed to simplify measurement of the resistive properties of semiconductor wafers and resistive films. It digitally computes and directly displays V/I, sheet resistivity, slice resistivity, or thickness as desired. It features a single compact package which incorporates both the probe mechanism and display. The rugged cast aluminum case assures mechanical integrity of the probe mechanism and coupled with compliant feet helps to reduce the adverse effects of vibration. The selected measured quantity is calculated and displayed digitally. The last measurement continues to be displayed until a new measurement is made, thus simplifing data recording.

Automatic ranging and automatic zeroing results in maximum operator convenience, and minimizes the possibility of operator error.

An indexing substrate holder allows repeatable probe positioning. A unique spring balance mechanization results in easily adjusted and repeatable probe pressures. Plug in adaptors simplify the changing of probe heads and adaptors are available for all commercially available units. RFI (radio frequency interference) and light effects on high resistivity semiconductor materials are minimized by an integral light and RFI shield.

The probe tips are unpowered until contact is made and probe

lowering is viscous damped. A measurement is automatically made each time the probe is lowered. Additional measurements can be made without lifting the probe by depressing a RETEST button. Pressing of the REVERSE current button will also produce an additional measurement except that in this case the direction of the test current is reversed. A questionable or invalid test is indicated by a flashing display. The maximum measureable sheet resistivity is 99.9 KΩ/sq. and the highest resolution is .01 mΩ/sq. Resolution of the digital display is maintained between .5 and .05% except for sheet resistivities below 2. mΩ/sq. The test current is continuously variable as an inverse function of the actual sheet resistivity. This eliminates the factor of 10 step change in test current which normally occurs at the range switch point and allows an optimum compromise between minimizing test current and maximizing signal level.

An FET input amplifier assures very low bias currents and true ratio measurement eliminates the need for accurate voltage reference and an accurate current source.

The slice or layer thickness necessary to compute the bulk resistivity of a slice or layer is inputed through digital thumbwheel switches in units of mils or microns. The unit will also display metalization thickness directly in KÅ if the bulk resistivity of the metal film is supplied.

The unit will automatically perform a semiconductor type test if desired. A rectification test is tried first. If the results

are inconclusive a thermoelectric test is attempted. If the result is still inconclusive a flashing display indicates that the sample type could not be determined.

If desired, the unit will supply a short low energy, high voltage pulse to the probe tips in order to penetrate any thin insulating layer on the sample. Both penetration and typing tests are only performed if activated by front panel switches. Both can be individually disabled internally if their inadvertant application would be detrimental to the sample.

1.2 OPERATION. The FPP-100 is normally supplied with a probe head mounted and the probe pressure adjusted to the probe head manufacturer's recommended value. If a different probe pressure is desired it is simply accomplished by adjusting the calibrated probe pressure adjustment screw. No special equipment is required.

The quantity to be measured must now be selected by depressing one of the four mode select switches. The unit will display sheet resistivity in Ω/sq, V/I in Ω, slice resistivity in Ωcm, or thickness in KÅ. If the slice resistivity is desired the thickness of the slice or layer must be inputed by means of the digital thumbwheel switches. Failure to select a thickness multiplier (x 1, 10 Mil, x 1, 10, 100μ) will result in a blank display multiplier (KΩ, Ω, mΩ, KÅ).

If thickness is desired the bulk resistivity of the film or layer must be inputed. Failure to select a bulk resistivity multiplier

(x 1μΩcm, x 10μΩcm, x 100μΩcm) will again result in a blank display multiplier.

If application of the penetrate voltage is desired on the following test, and on the following test only, the PENETRATE SINGLE button should be depressed. This will illuminate the PENETRATE light. Illumination of the PENETRATE light indicates that a penetrate will be performed on the following test. If a penetrate is desired each time the probe is lowered the PENETRATE AUTO switch should be depressed. This is a latching switch and will remain depressed until it is pushed again. If a type test is desired, one of the TYPE switches should be depressed. Again if a type test is desired each time the probe is lowered the TYPE AUTO switch should be depressed. If the type test is desired only on the following probing the TYPE SINGLE switch should be depressed. Illumination of the TYPE light indicates that a type test will be performed on the next probing.

In the event that either of these functions was inadvertantly selected and it is undesirable to perform the function, the unit can be cleared by turning the power off for three seconds and then back on again.

After the desired measurement and functions are selected the sample is dropped into the sample holder and the holder slid into the desired probing position. Lowering of the probe onto the sample can be accomplished by depressing the actuator bar or by closing the cover. For high resistivity samples which may be affected by light or in which

the reading may be affected by RFI it is suggested that the cover be closed.

Upon lowering of the probe the FPP-100 display will go blank for a short period of time (typically one sec., a maximum of 2 sec.) after which the desired measurement will be displayed with a properly positioned decimal point and display multiplier. The probe actuator must be depressed or the cover closed throughout the blanked display period or the measurement will be aborted. Flashing of the total display indicates an aborted measurement. Flashing of the display multiplier indicates a measured value beyond the display capability of the unit. Inability to determine the semiconductor type will result in a flashing of the P and N indicators if a type test was performed.

If a second measurement is desired prior to lifting the probe this can be initiated by momentarily depressing the RETEST button. If a second measurement with the test current reversed is desired it can be initiated by momentarily depressing the REV CURR button.

1.3 FEATURES AND SPECIFICATIONS.

1.3.1 FEATURES.

- Compact integral probe and display.
- Digital display and computation.
- Automatic ranging.
- Four selectable displays.
    a. Sheet resistivity.
    b. V/I.
    c. Slice resistivity (bulk resistivity of a slice of known thickness)

d. Metalization thickness (displayed directly in KÅ)

- Digital input of slice thickness or bulk resistivity.
- Automatically makes measurement each time probe is lowered.
- Retest and Reverse push buttons allow additional measurements without disturbing probes.
- Automatically holds last reading after probe is released and until next measurement is made.
- Flashing display indicates questionable or invalid test.
- Extended measurement range.
  Displays sheet resistivity up to 100 KΩ/sq.
  Displays sheet resistivity resolution down to .01 mΩ/sq.
- High accuracy of ±.5% of reading on all but extreme ranges.
  Unique auto zero circuit minimizes thermal and source impedance effects.
  FET input amplifier features low bias current.
  Continuously variable test current allows test current to be minimized consistant with an acceptable signal to noise ratio.
  True ratio measurement.
- Integral RFI and light shield for high resistivity measurements.
- Unique "constant force" spring balance system assures repeatable probe pressure.
- Probe pressure conveniently set by means of calibrated adjustment knob.
- Plug-in probe head adaptors make probe head changing convenient and non-cirtical.
- Unique, indexed substrate holder allows semi-repeatable probe positioning on substrate.
- Probe head is viscously lowered.
- Heavy base and compliant feet minimize susceptibility to vibration.
- Automatic determination of semiconductor type if desired.
  Automatically utilizes either rectification or thermoelectric typing as required.
- Automatic penetration if desired.
- Penetration and typing modes can be individually disabled by means of internal switches.

- o Very low power requirement.
- o No batteries required.

1.3.2 MECHANICAL SPECIFICATIONS.

Probe Head:

The FPP-100 can be supplied with any of the commonly available probe heads. A readily removable plug-in probe head adapter is available for any of the commercially available probe heads which makes changing of the probe head easy and non-critical.

Probe Mechanism:

Mechanism Type:
Parallel beam with flexural pivots. Probe force established by a unique constant force spring balance system.

Probe Force Adjustment Range:
0 to 200 gm/pin.

Probe Force Calibration Accuracy:
$\pm$5% or $\pm$2 gm whichever is greater.*

Probe Force Variation With Height:
Less than 0.2 gm/mil.**

* Refers to the total of all four pins. Pin to pin force variation is controlled by the probe head manufacture.
** Average per pin force.

Size: 12.5" wide x 11.0" deep x 6.3" high.

Weight: 15 lbs.

1.3.3 ELECTRICAL SPECIFICATIONS:

Measurement Modes and Ranges:

MODE	MULTIPLIER	RANGE MINIMUM	RANGE MAXIMUM
Sheet Resistivity	Don't Care/Geom. Corr.	0.00 mΩ/sq.	99.9 KΩ/sq.
Slice Resistivity	1.0 to 9.99 mil	.000 mΩ cm	.45 to 4.5 KΩ cm
	10 to 99.9 mil	0.00 mΩ cm	4.5 to 45.0 KΩ cm
	1.0 to 9.99 μ	1.000 to .250 mΩ cm	99.9 Ω cm
	10 to 99.9 μ	1.000 to .250 mΩ cm	999. Ω cm
	100 to 999. μ	.000 mΩ cm	9.99 KΩ cm
Thickness	1.00 to 9.99 μΩ cm	.250 to 1.000 KÅ	4.50 to 45.0 KÅ
	10.0 to 99.9 μΩ cm	.250 to 1.000 KÅ	45.0 to 450. KÅ
	100 to 999. μΩ cm	.250 to 1.000 KÅ	450. to 999. KÅ
V/I	Don't Care/Geom. Corr.	0.00 mΩ	40.0 KΩ

Resolution: With the exception of the minimum range the resolution of the display is maintained between 0.5% and 0.05% of reading.

Overall Accuracy*

Accuracy for sheet resistance between 20 mil Ω/sq. and 20 KΩ/sq.

±0.5% of reading	90 days
±1.0% of reading	1 year

Accuracy for sheet resistance greater than 20 K Ω/sq.

±2% of reading	90 days
±5% of reading	1 year

Accuracy for sheet resistance less than 20 mil Ω/sq.

±2% or ±0.1 mil	whichever is greater	90 days
±5% or ±0.2 mil	whichever is greater	1 year

Conditions:

Temperature range:	15°C. to 35°C., 60°F. to 95°F.
Relative humidity:	less than 50%.

* Exclusive of probe errors.

Current probe contact resistance: less than 1000 times V/I.

Voltage probe contact resistance: less than 100 kilohm.

(See voltage detector characteristics for effect of voltage probe contact resistances above 100 kilohm.)

Current Source Characteristics:

Nominal current as a function of sheet resistance:

$$I^* = \frac{45.3\ mV}{\text{Sheet resistance in ohms}} \quad \pm 10\%$$

Nominal current as a function of V/I:

$$I^* = \frac{10mV}{V/I \text{ in ohms}} \quad \pm 10\%$$

* I reduced by 1/2 for thickness measurement.

Range: Less than 400 μa to greater than 400 ma.

Compliance: The current source voltage compliance varies with current per the following table:

Sheet Resistivity Range	Maximum Test Current	Minimum Compliance Voltage
greater than 100 ohm/sq.	453 μa	40 volts
10 to 100 ohm/sq.	4.53 ma	16 volts
1 to 10 ohm/sq.	45.3 ma	12 volts
.1 to 1 ohm/sq.	453 ma	3 volts
less than .1 ohm/sq.	500 ma	2.5 volts

Voltage Detector Characteristics:

Input impedance: 10^{+12} ohm or greater

Input bias current: 15 pA typ., 50 pA maximum

Accuracy degradation less than:

.1% for contact resistance less than 100 kilohm.

3% for contact resistance less than 1 megohm.

Typing Mode Characteristics:

·Applied voltage: 14 Vrms ±20%

Source resistance: 18 ohm ±20%

Detection level,

Rectification: 0.5 VDC

Thermoelectric: 0.5 mVDC

Can be selected to occur automatically with each test, or singly on the next test, or not at all. Can be internally disabled independently of front panel selection if desired.

Penetration Mode Characteristics:

Voltage: 170 volts ±20%

Source Resistivity: 10 megohm ±20%

Duration: 4 milliseconds ±20%

Can be selected to occur automatically with each test, or singly on the next test, or not at all. Can be internally disabled independently of the front panel selection.

Power Requirements:

115/230 V ±10%

50/60 Hz

Approximately 10 watts

Operating Temperature Range:

15°C to 35°C

60°F to 95°F

SECTION 2

FRONT PANEL CONTROLS AND INDICATORS
(REF. FIGURE 2.0)

2.1 POWER ON SWITCH. Turns power on.

2.2 MODE SELECT SWITCHES. These four switches are mechanically interlocked so that only one can be depressed at any one time.

a. SHT. RES switch
Puts unit into sheet resistivity mode. Unit calculates and displays sheet resistivity based on measured V/I.

b. SLICE RES switch
Puts unit into slice resistivity mode. Unit calculates and displays the bulk resistivity of a slice or sheet of material whose thickness is entered into the unit by means of the THICKNESS/RESISTIVITY thumbwheel switches.

c. V/I switch
Puts unit into V/I mode. Unit displays measured V/I.

d. THK switch
Puts unit into thickness mode. Unit calculates and displays the thickness of a slice or sheet whose bulk resistivity is entered into the unit by means of the THICKNESS/RESISTIVITY thumbwheel switches.

2.3 PENETRATION SWITCHES.

These switches determine whether the unit will perform a penetrate action on subsequent probings.

SINGLE: This switch is a momentary switch and depression of it will illuminate the PENETRATE light and cause the unit to perform a penetrate on the next probe cycle and the next probe cycle only, after which the PENETRATE light will go out.

FIGURE 2.0 FPP-100 FRONT PANEL

AUTO: This switch is a push-on/push-off switch and pressing it on will light the PENETRATE light and cause the unit to perform a penetrate automatically on each probe cycle until it is pushed off.

PENETRATION Light

An ON condition of the PENETRATION light indicates that a PENETRATION test will be performed on the next probe cycle.

2.4 TYPE SWITCHES. These switches determine whether the unit will perform a type test on subsequent probings.

SINGLE: This switch is a momentary switch and depression of it will illuminate the TYPE light and cause the unit to perform a type on the next probe cycle and the next probe cycle only, after which the TYPE light will go out.

AUTO: This switch is a push-on/push-off switch and pressing it on will light the TYPE light and cause the unit to perform a type automatically on each probe cycle until it is pushed off.

TYPE Light

An ON condition of the TYPE light indicates that a TYPE test will be performed on the next probe cycle.

2.5 RETEST SWITCH. The RETEST switch is a momentary switch. Momentary depression of this switch will initiate an additional test if the probe has been held down. Continuous depression of this switch will cause continuous tests.

2.6 REV CURR SWITCH. The REV CURR switch is also momentary and depression of it will initiate an additional test with the test current reversed. Continuous depression will produce repeated measurements with the test current always in a direction opposite to that of a normal test or a retest.

2.7 THICKNESS/OHMS DISPLAY. The THICKNESS/OHMS display has a total of four digits, however, the fourth digit is only displayed when the most significant digit is one and then it is noticeably dimmer than the other digits. This is done so that undue significance will not be attributed to this digit as it is generally displaying a resolution beyond the basic accuracy of the unit, or for that matter the probing process. The flashing of this display indicates a questionable or invalid measurement.

The units of the display are indicated by illuminating the LED next to the appropriate units designator. The KΩ, Ω, and mΩ designators are assumed to be Ω/sq. for a sheet resistivity measurement Ωcm for a slice resistivity measurement and Ω for a V/I measurement. Some combinations of inputs can result in a measurement which lies outside of the display range. This condition is indicated by flashing the units designator.

2.8 OVERRANGE INDICATOR. Illumination of this light emitting diode indicates that the sample has a sheet resistivity greater than the measurement capability of the unit, or in the thickness measurement mode an I/V greater than the measurement capability of the unit.

2.9 TYPE INDICATORS. The N and P indicators are illuminated only after a type test. Illumination of the P LED indicates P type material. Illumination of the N LED indicated N type material. Flashing of both the N and P indicators occurs if the results of the typing test were inconclusive.

2.10 THICKNESS/RESISTIVITY THUMBWHEEL SWITCHES. These switches are used to input the necessary thickness or bulk resistivity information needed in the slice resistivity or thickness measurement modes.

The first three digits determine the magnitude and are limited in range from 1.00 to 9.99. ie: Zero to the left of the decimal point is not allowed and stops in the switch eliminate this possibility.

The last switch is refered to as the message multiplier and defines the units and decade multipliers if applicable.

2.11 GEOM. CORR. (GEOMETRIC CORRECTION). In some extreme cases it might be desirable to multiply the measured result times a geometric correction. This correction, as discussed in Technical Papers, [1,2] generally has to do with the ratio of the diameter of the wafer (D) divided by the probe spacing (S). If the resultant number (D/S) is greater than 40, no correction is necessary. For D/S values less than 40 typical configurations of wafer diameter (D) and probe spacing (S) are indicated on Figure 2.1 along with a plot of the same information on Figure 2.2. For sheet and V/I measurements you input the correction by selecting the Geom. Corr. message and inputting the correction directly on the three decades of thumbwheel switches, disregarding the decimal point on the switch.

Example: If the probe spacing is 62.5 mils, and the wafer is 1.0 in. in diameter then $\frac{D}{S} = \frac{1000}{62.5} = 16$. From Figure 2.1 or 2.2 the correction factor for 16 is .967. Enter 967 on the thumbwheel switch, along with Geom. Corr. message. The resultant display will be multiplied by .967

thus compensating for the geometry error. For thickness or slice function, multiply the ohms/cm or thickness by the correction factor.

GEOMETRIC CORRECTIONS

25 MIL PROBE SPACING (S)

DIA (D)	D/S	CORRECTION	% ERROR
1.00	40	.995	+.5%
1.5	60	1.00	0
2.0	80	1.00	0
3.0	120	1.00	0

40 MIL PROBE SPACING (S)

DIA (D)	D/S	CORRECTION	% ERROR
1.0	25	.985	+1.5%
1.5	37.5	.994	+.6%
2.0	50	1.00	0
3.0	75	1.00	0

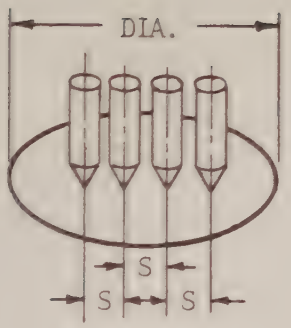
62.5 MIL PROBE SPACING (S)

DIA (D)	D/S	CORRECTION	% ERROR
1.0	16	.967	+2.3%
1.5	24	.985	+1.5%
2.0	32	.991	+.9%
3.0	48	1.00	0

FIGURE 2.1.

[1] Valdes, L. B., Resistivity Measurements on Germanium for Transistors, Proc. of I.R.E., 42, February, 1954, p. 420.
[2] Smits, F. M., Measurement of Sheet Resistivities with the Four Point Probe, The Bell System Technical Journal, May 1958, p, 711.

D/S	CORR.
∞	1.00
40	.995
20	.979
15	.963
10	.920
7.5	.866
5.0	.742
4.0	.646
3.0	.500



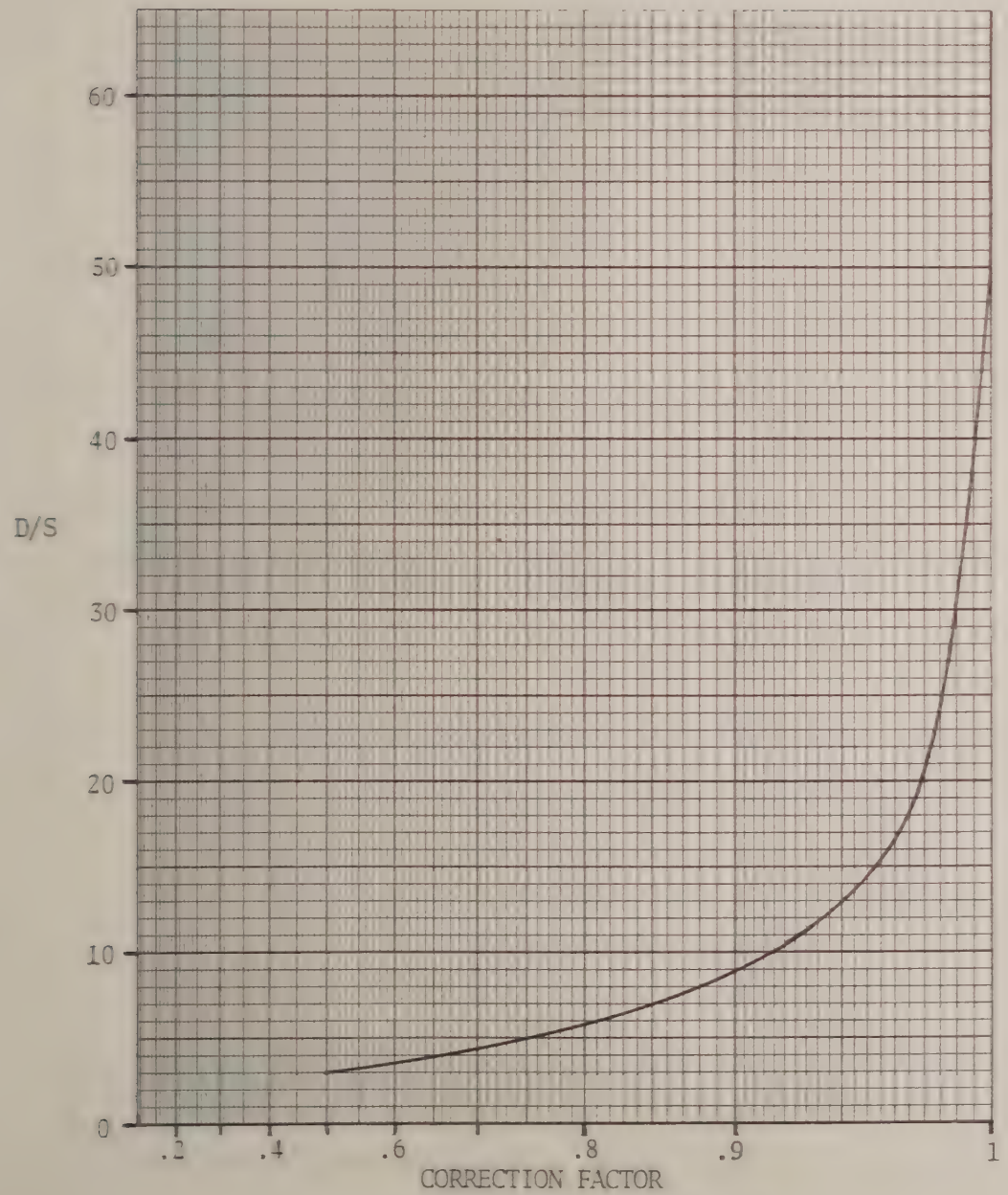


FIGURE 2.2 GEOMETRY CORRECTION

SECTION 3

INSTALLATION

3.1 UNPACKING AND INSPECTION. The FPP-100 is shipped in a special shipping carton, which should be saved if reshipment is anticipated. The inserts hold the unit securely in the carton and absorb any reasonable external shocks normally encountered in transit. Prior to unpacking, examine the exterior of the shipping carton for any signs of damage. Carefully remove the FPP-100 from the carton and inspect the exterior of the instrument for any signs of damage. If damage is found a claim should be filed with the carrier and a copy forwarded to VEECO/Kronos. If the unit is to be returned for inspection, repair, or calibration, authorization must be obtained from VEECO/Kronos prior to return. Should the unit fail to function properly, or fail to meet any of its specifications, contact your local VEECO Sales/Service Representative, or the Technical Service Department, VEECO INSTRUMENTS, Terminal Dr., Plainview, N.Y. 11803, (516) 681-8300.

3.2 LINE VOLTAGE. This equipment is normally factory set for operation on a 115 VAC, 60 Hz line unless otherwise requested. It is good practice to check that the setting of the 115/230 volt line switch on the rear panel is set to your line voltage before proceeding with pre-installation or permanent installation.

Do not connect to a 230 volt line if unit is set for 115 volt operation, as damage will result.

To change the setting of the switch on the rear panel, Figure 3.1, insert the blade of a small screwdriver in the slot provided and slide the switch all the way in the direction required.

NOTE: Connect the FPP-100 to a power line with an adequate ground. Never operate the FPP-100 ungrounded.

3.3 PRE-INSTALLATION CHECKOUT (FUNCTIONAL TEST). The FPP-100 has been electrically tested and calibrated prior to shipment. The FPP-100 can be functionally checked by the following procedure.

a. Place the unit on a convenient work bench.

b. Check that the power is off.

c. If the probe is installed loosen the two screws which secure the probe adaptor to the FPP-100. Remove the probe assembly by sliding it forward thus disconnecting the probe connection to the FPP-100 housing, Ref. Figure 3.2.

d. Caretully remove the bottom cover, unsnap the probe simulation cable from its holderd, Ref. Figure 3.3, and connect it to the probe mating connector, Ref. Figure 3.4.

e. Connect a resistor (0.00 mΩ to 40.0 KΩ) to the binding posts on the rear panel of the FPP-100 as indicated in Figure 3.5.

f. Turn power on.

g. Select V/I.

h. Press the actuator bar down and hold it down. The display should go blank for approximately one second and then display the resistor value directly.

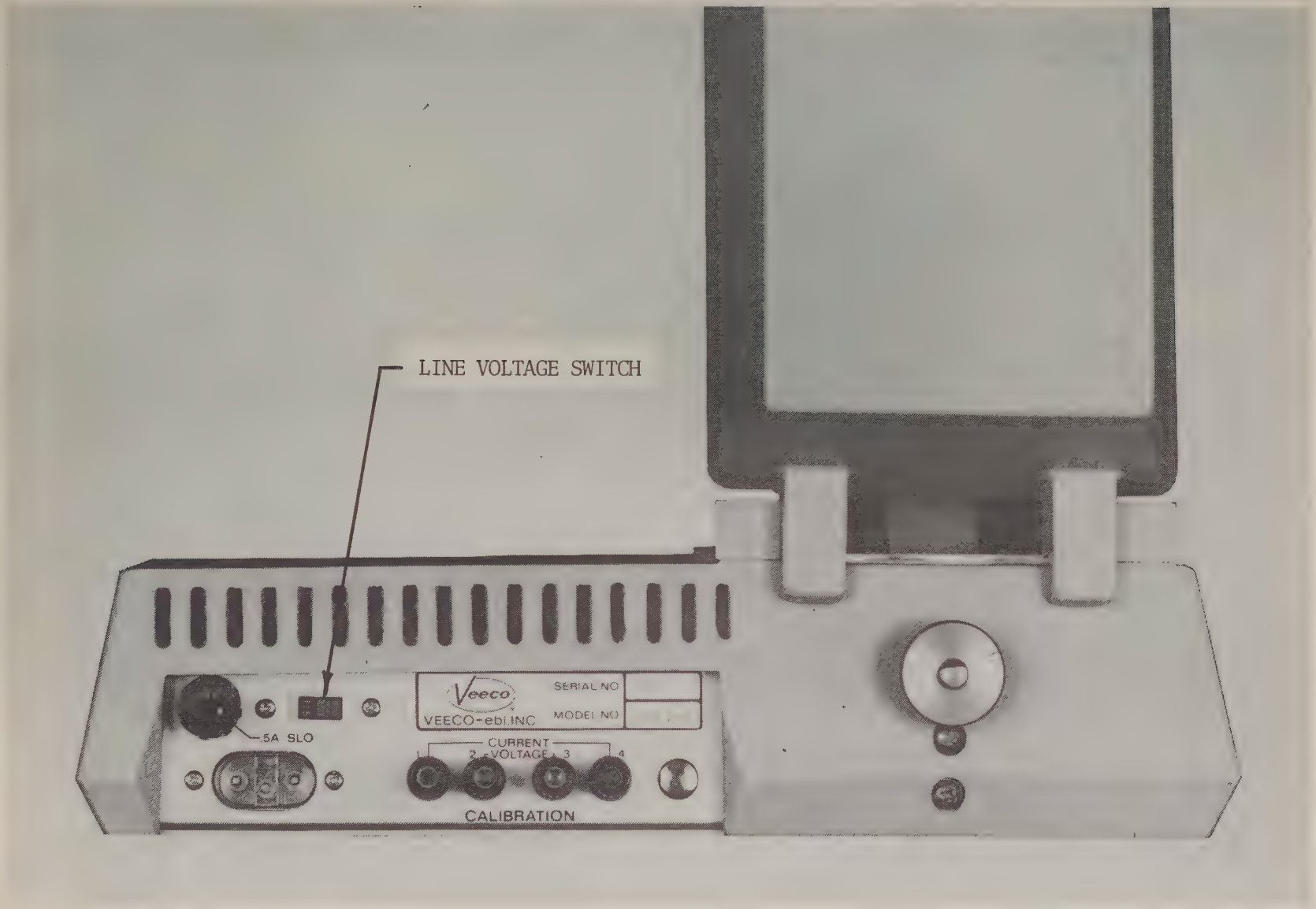


FIGURE 3.1 FPP-100 REAR PANEL

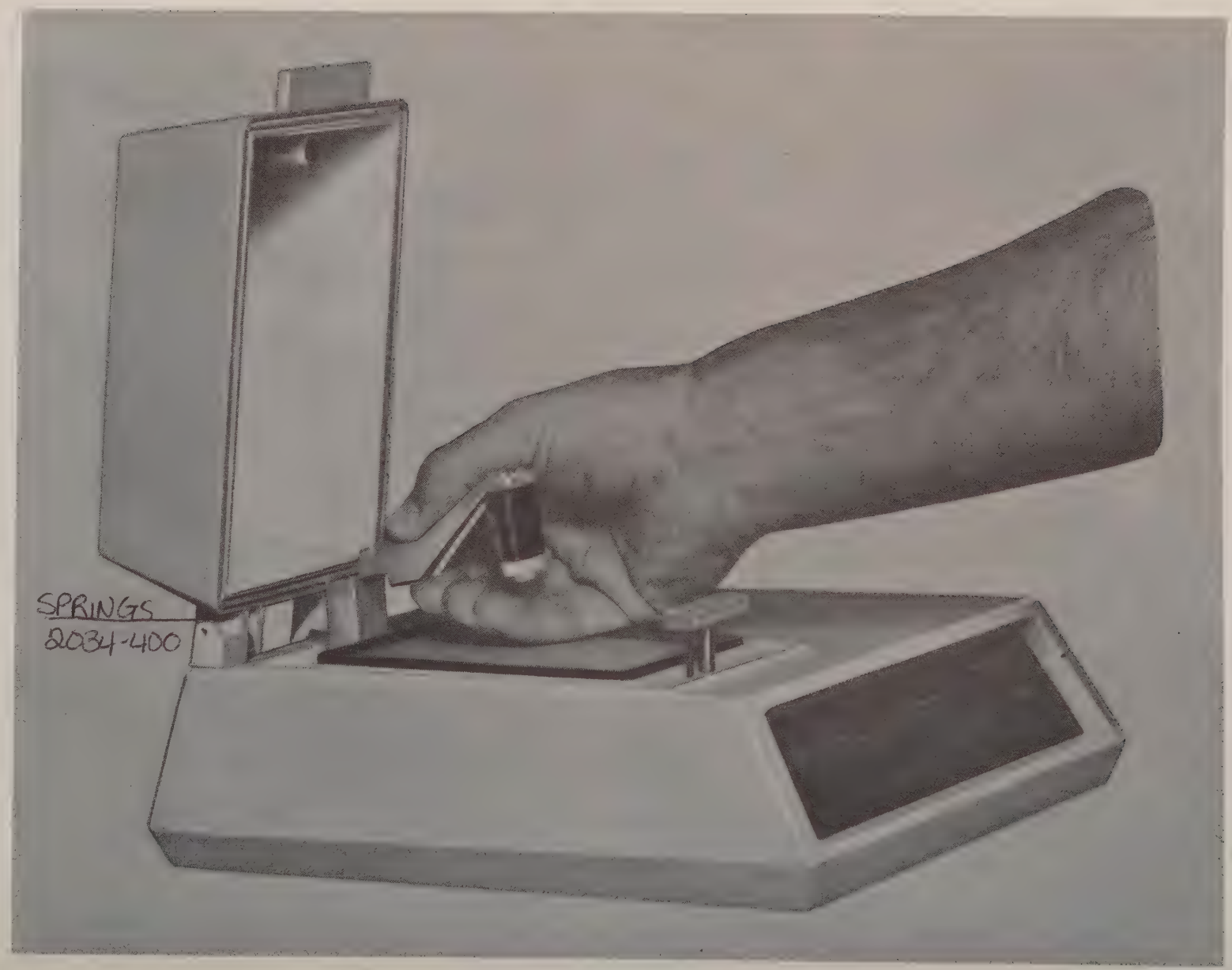


FIGURE 3.2 PROBE HEAD REMOVAL

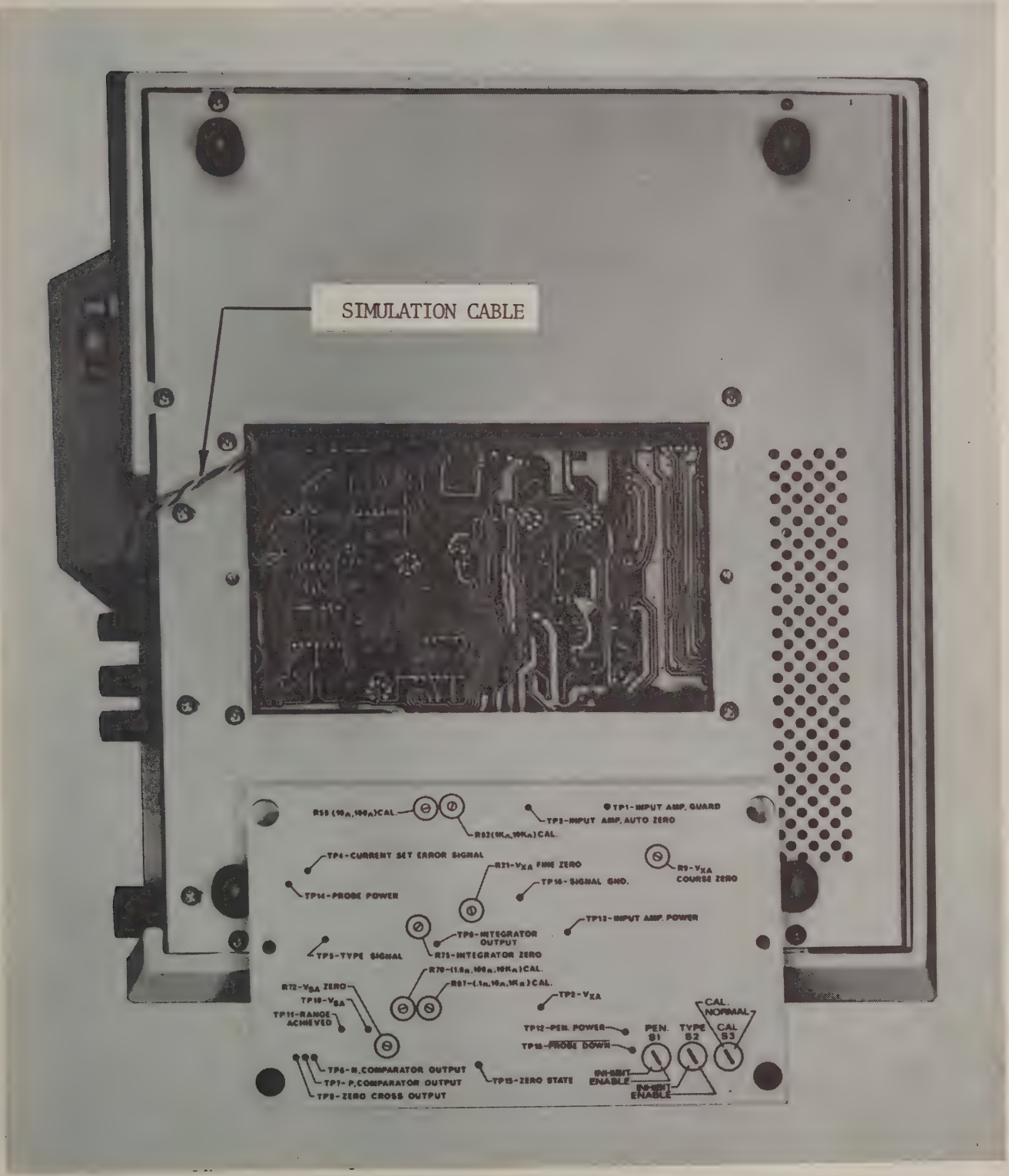


FIGURE 3.3 BOTTOM COVER REMOVED

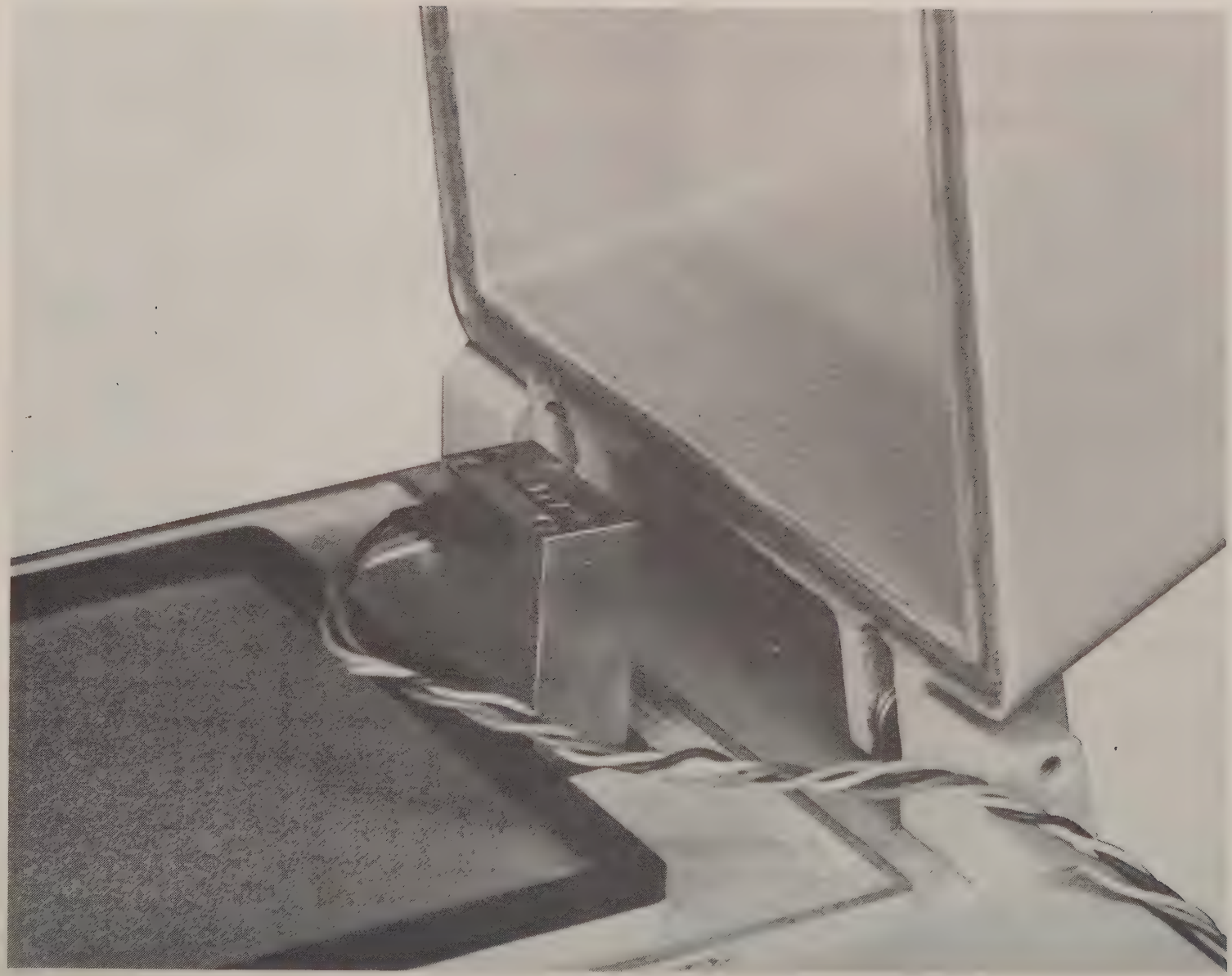


FIGURE 3.4 PROBE SIMULATION CABLE INSTALLATION

i. The unit is now configured as a digital ohm meter with an actual range from 0.00 milliohm to 40.0 kilohm, with .5% overall accuracy or ±1 digit whichever is greater. Any resistance values between the above range can be checked. Should an actual calibration be required refer to Section 7.4.

j. If the FPP-100 was shipped without a probe, refer to Section 7.3 on probe installation.

k. Reinstall probe assembly. The unit is ready for operation.

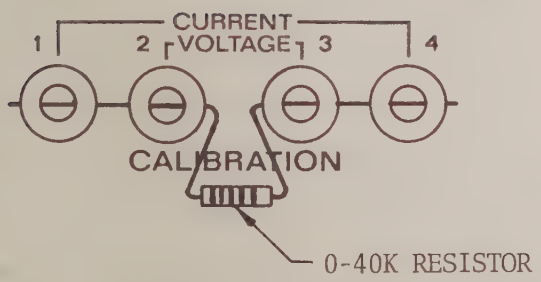


Figure 3.5

SECTION 4

OPERATING INSTRUCTIONS

4.1 BASIC TEST STATION. The FPP-100 is a compact integrated four point probe test station incorporating easily replaceable probe head adaptor assembly, probe mount and constant force lowering mechanism, pre-indexed wafer carrier, RFI light shield, solid state electronics and LED display. As shipped the FPP-100 is ready to plug in, turn on, and test your 2 or 3 inch fragmented wafers, epitaxial diffused ion implanted layers or metallization.

4.2 ADJUSTMENT OF PROBE FORCE. The probe can be adjusted from 0 to 200 grams per pin. This adjustment should be made in accordance with the probe head manufacturers specification and past history of probing. The probe force is adjusted by turning the calibration knob on the rear of the instrument to the desired force as indicated on the calibrated shaft. The calibrated shaft is indexed in 20 gram increments, and the calibration knob is indexed in 1 gram increments, or 5 grams per revolution. See Section 7, paragraph 7.5 for procedures required to change probe head types.

4.3 MODE SELECTION. Proper mode selection should be determined prior to probing. The following describes the FPP-100 input modes and functions:

a. V/I Function. The unit will display V/I (ohms) directly.

b. Sheet Resistivity Function. The unit will display sheet resistivity (ohms/sq.) directly, based on V/I measurement.

c. Slice Resistivity Function. The unit will display the bulk resistivity of a slice or sheet of material. The thickness of the material must be entered into the unit by means of the thickness/resistivity thumbwheel switch and multiplier message. The thickness can be entered in mils or microns. If the material thickness is not entered properly there will be no decimal point on multiplier displayed. If the mΩ indicator is flashing, the reading is beyond the range of the instrument.

d. Thickness Function. The unit will display actual thickness in KÅ. The bulk resistivity of the material (ohm-cm) must be entered into the unit by means of the thickness/resistivity thumbwheel switch and multiplier message. If the bulk resistivity is not entered properly there will be no decimal point or multiplier displayed. For measurements beyond the range of the instrument the KÅ. indicator will flash.

4.4 PENETRATION FUNCTION AUTO/SINGLE. A high voltage low energy pulse is applied to the probe tips in order to penetrate any thin insulating layer on the sample. If the "single" penetration is selected, the penetrate indicator will light indicating a penetrate will be performed on the next cycle. If "auto" penetrate is

selected, the unit will penetrate every cycle. The penetrate function can be inhibited completely by changing the position of the penetrate enable switch. This switch is accessible from the bottom of the instrument (ref figure 4.1).

4.5 TYPING FUNCTION, AUTO/SINGLE. If "single" type is selected, the type indicator light indicates typing will be performed on the next cycle. If "auto" type is selected, typing will be performed on each cycle. If both N and P indicators flash, this indicates the unit was unable to type the sample. The "type" function can be inhibited completely by changing the position of the type enable switch. This switch is accessible from the bottom of the instrument (ref. figure 4.1).

4.6 PROBING.

a. Place the wafer on molded wafer carrier. Lining up flatted edge with the carrier. The carrier will index to one of five detent positions.

b. Select proper mode, as described in 4.3.

c. Turn power on.

d. Close RFI light shield to initiate test. The display will go blank for not more than 2 sec at which time the display will appear. By depressing the Retest button you can reinitiate the test. By depressing the Rev Curr button you can reinitiate the test with the test current reversed. If the digital display is flashing, this indicates the probe was not down for the machine cycle, and an additional test should be made.

e. Probing can be accomplished by depressing the actuator bar down, without closing the RFI light shield.

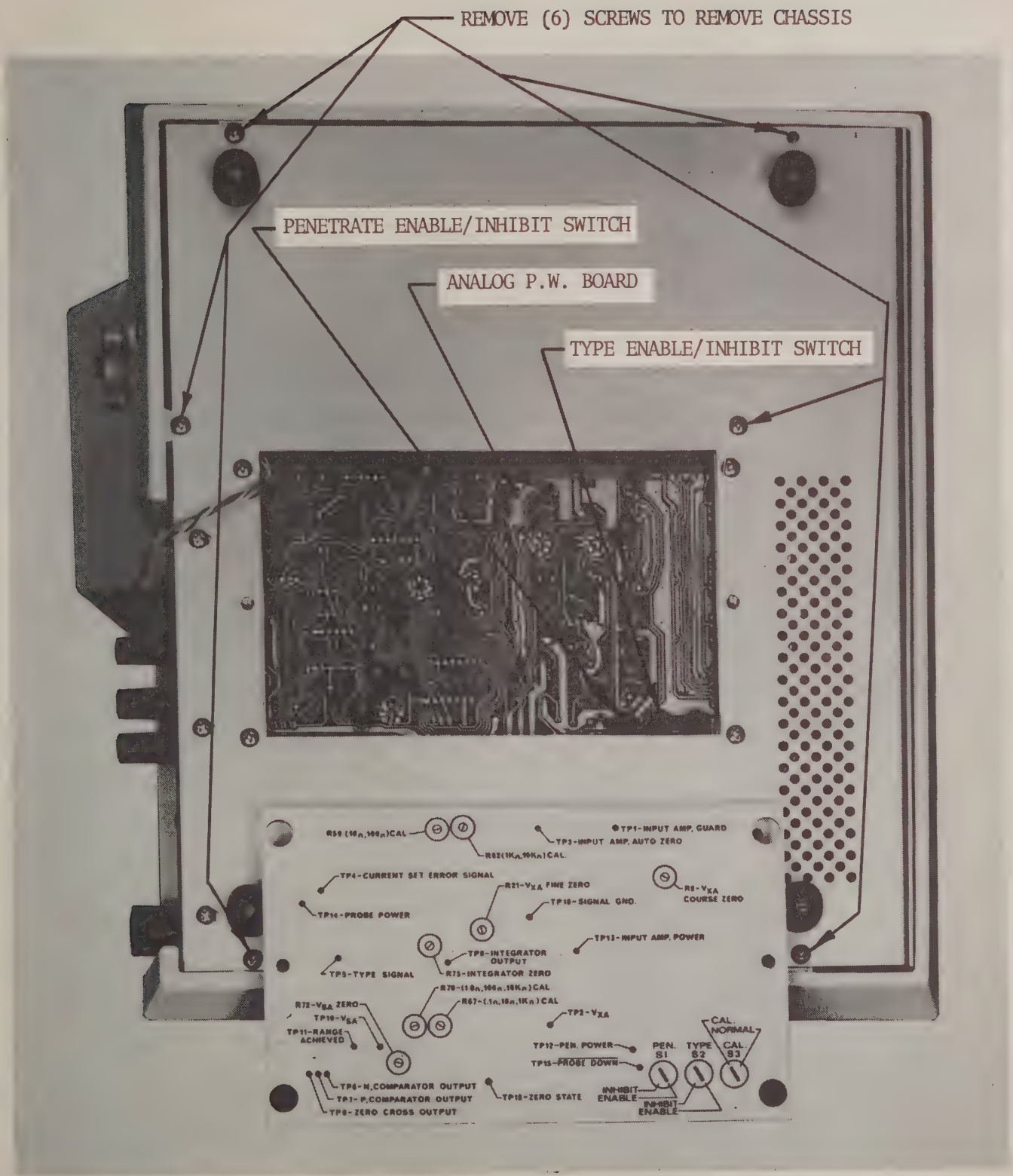


FIGURE 4.1 CALIBRATION COVER & CHASSIS REMOVAL

SECTION 5

THEORY OF OPERATION

5.1 RESISTIVITY MEASUREMENTS UTILIZING A FOUR POINT PROBE. The four point probe is an effective means of measuring the sheet resistivity of thin resistive films. The sheet resistivity of a film is defined as the resistance that would be measured between two electrodes placed on opposite edges of a square of the film. As long as the film is square (has equal edges) the measured resistance is independent of the size of the square.

That this is so becomes intuitively obvious if one considers a square subdivided into four smaller squares. The large square can then be thought of two series legs (each two squares long) connected in parallel. If the small square has a resistance X then the series legs each have a resistance of 2X. The resistance of the two series legs connected in parallel must be $\frac{2X}{2}$ or X. Thus we see that the edge to edge resistance of the large square is the same as the edge to edge resistance of the small squares. Specifically the sheet resistivity of a film is independent of size and has dimensions of ohms only. In order to indicate that the quantity is a sheet resistivity rather than the resistance of a two terminal device it is refered to as Ω/sq. is a dimensionless quantity. The four point probe most commonly used for measuring resistivity consists of four points placed in a straight line (a linear array) and equally spaced. Current is forced to flow between the outer probe points and the voltage developed in the film

by this current is picked up by the inner probe points. Assuming that the film is thin (much thinner than the probe spacing) and larger in area (much larger than the probe spacing) a theoretical relationship can be derived which relates the sheet resistivity with the ratio of the inner probe voltage to the outer probe current. This relationship is independent of probe spacing (provided the spacing between each probe point is equal) and independent of probe point contact resistance (provided that no current flows in the voltage (inner) probes. The equation relating sheet resistivity and V/I is given below.

$$\text{Sheet resistance} = \left(\frac{\pi}{\ell n\ 2}\right)(V/I) = 4.5324\ (V/I)$$

Any resistive sheet is in reality a sheet of bulk material. If the bulk resistivity of the material is constant (independent of the distance from the surfaces), and the thickness of the film or sheet is W, then the resistivity of the sheet is related to the thickness and the bulk resistivity of the film by the following equation.

$$\text{Sheet resistivity} = \frac{\text{bulk resistivity}}{\text{thickness}} = \frac{\text{bulk}}{W}$$

If the bulk resistivity is expressed in ohm centimeters (the most commonly used units) the thickness, W, must be expressed in centimeters.

From the above expression we can derive expressions for bulk resistivity as a function of sheet resistivity and thickness and for thickness as a function of sheet resistivity and bulk resistivity.

$$\text{Slice resistivity} = \rho\,\text{slice} = \rho\,\text{sheet}$$

$$\text{Sheet thickness} = \rho\,\text{sheet}$$

In order to indicate that the displayed bulk resistivity is calculated from the measured sheet resistivity and a knowledge of the sheet

thickness, the bulk resistivity of the sheet is referred to as the slice resistivity, ρ slice.

A true bulk resistivity measurement (one in which the dimensions of the bulk material are much larger than the probe point spacing) can be made with a four point probe, however, in this case the spacing of the probes enters directly into the relationship between V/I and ρ bulk. The FPP-100 is designed for probing thin substrate and therefore does not have this capability.

5.2 BASIC OPERATION OF THE FPP-100. Initiation of the measurement cycle of the FPP-100 is affected by depressing the actuation bar which connects the Probe Down signal line to ground. This action occurs at the end of the actuator bar travel. The display is blanked throughout the measurement cycle and the probe actuator must be held down throughout this period or the measurement will be aborted. An aborted measurement will be indicated by a flashing display.

Following closure of the Probe Down signal to ground there is a 256 msec delay before any action is initiated. This assures that the probe is on and stable. If a penetrate function is called for this is accomplished immediately after the delay by closing a 4 pole reed relay which applies 170 volts through 10 MΩ resistors to the probe pins. This relay is closed for only 4 msec.

256+5 = 261 MSEC

One msec after the penetrate relay opens, or 5 msec after the probe down delay if no penetrate was performed, a 4 pole reed relay is closed to connect the probe pins to the resistivity measuring circuitry. The first 128 msec of the resistivity measurement cycle is used to zero the

DELAY CONNECT ZERO

input voltage amplifier and the current sense amplifier. It is significant that the input amplifier is zeroed with the probe pins in contact on the test specimen. This assures that the readings will not be effected by varying contact potentials. Zero test current is assured during this period by keeping open a reed relay in series with the test current supply.

389 msec after PROBE DOWN to ground (PRDN) I_X

After zeroing, the I_x (test current) relay is closed and the test current is brought up to a level which results in an inner probe voltage of 10 mV (5 mV in the thickness measurement mode). The time allowed to establish current is 64 msec. 453 msec after PD. The maximum test current is limited to 500 ma so that for very low sheet resistivity the inner probe voltage may not reach 10 mV. This is not significant however, because it is the voltage to current ratio V/I that is measured not the absolute values of voltage or current.

453 msec after PD

Following establishment of the test current the shunt is ranged. This is accomplished by increasing the shunt value by a factor of 10 every 64 msec until the output of the current sense circuit exceeds a minimum level or the maximum shunt value has been selected. NTE 500MA sensed by Current Sense Amplifier

Resulting in 10MV ON VOLTAGE SENSE 453 msec + N x 64 msec

After the range has been established the analog to digital conversion of the V/I ratio (I/V in the thickness mode) is accomplished. In order to assure adequate resolution in the display a trial conversion is first tried at 10 times the normal scale factor. If the result of this conversion is within range it is stored for future display and a second conversion is not made. If, however, the result of the first conversion is overrange a second conversion is accomplished with the scale factor reduced by a factor of 10. The second conversion will

always be in range (except at the extreme upper range of the FPP-100, (sheet resistivity greater than 100 KΩ/sq.) and will be stored for future display.

Following the V/I conversion the test current is reduced to zero and the four pole input reed relay is opened.

If a Type test is not called for, the FPP-100 now goes into the display state, displaying the measured quantity and indicating that the measurement cycle is complete and the actuator bar may be released.

If a Type test is called for a three pole reed relay is closed which connects three of the four probe pins to the type determining circuitry. The type power is applied to two adjacent pins on the probe. It is supplied for 256 msec at the end of which time any dc voltage developed on the third pin is sampled. If the magnitude of this voltage is sufficient the type is determined from the polarity of the voltage and is stored for later display. If the magnitude of the dc voltage is insufficient, immediately after the type power is removed (the three pole type relay is opened) the input amplifier is reconnected for 4 msec and the Seebeck voltage, if any, developed between a cold probe pin and one heated as a result of the former type power application is sampled. If this voltage is of sufficient magnitude its polarity determines the type which is stored for future display. If the magnitude of this voltage is insufficient to determine the semiconductor type this information is stored for later display as indecision on type.

At the conclusion of the type test all relays are open, the FPP-100 goes into the display state displaying the measured quantities and indicating that the actuator bar may be released.

5.3 GENERAL DESCRIPTION AND BLOCK DIAGRAM. Reference to the block diagram in figure 5.1 will aid in understanding the operation of the FPP-100.

The Probe Switch Network consists of five normally open reed relays which connect the four probe lines to the internal circuitry as required. The relays are normally open and indeed are only closed during the display blanking period.

The Current Source supplies the probe current during resistivity measurements. It is capable of supplying currents from less than 500 na to greater than 453 ma. It receives as a feedback signal the output of the input amplifier and adjusts the current it supplies until the feedback signal indicates that the inner probe voltage is 10 mV except in the thickness measurement mode where the current is established at a level which will result in an inner probe voltage of 5 mV.

The Current Sense Circuitry senses the probe current and converts it to a voltage signal. It consists of three current sensing resistors, a buffer amplifier with two gain configurations differing by a factor of 10, a zero sense and hold amplifier, a comparator and a number of solid state switches. The solid state switches are able to select one of six possible effective shunt values by selecting the proper

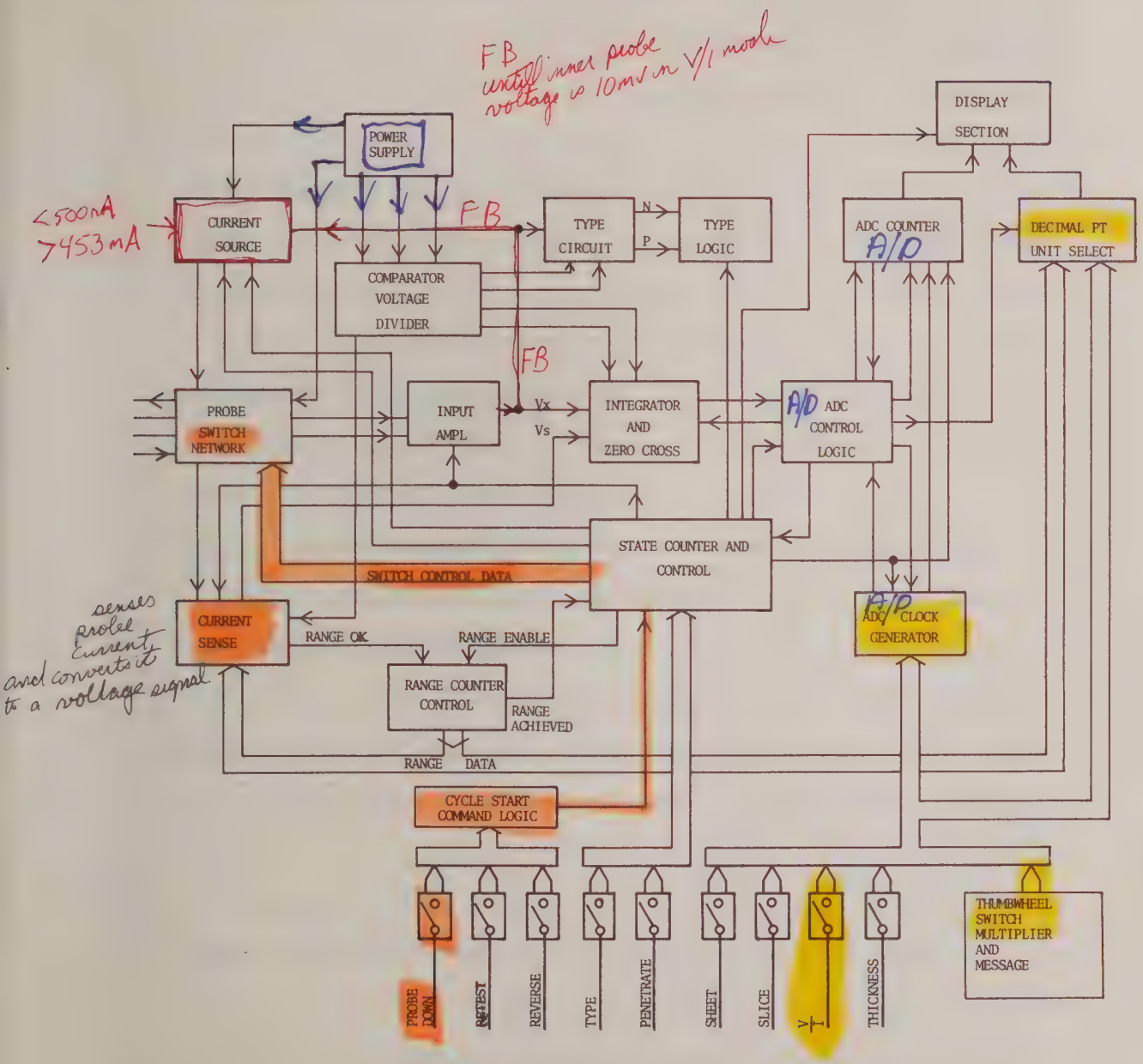


FIGURE 5.1 BLOCK DIAGRAM

resistor and the proper gain configuration. The zero sense and hold amplifier is used to drive the output of the buffer amplifier to zero prior to sensing current. The comparator signals that the buffer amplifier output is above some minimum value i.e. that the proper shunt range has been achieved.

The Range Counter Control supplies the drive signals to the solid state switches in the Current Sense circuit. On receipt of a signal from the state counter and control it sequentially steps the effective shunt valve from its minimum value to its maximum value or until a range OK signal from the Current Sense circuit indicates that the range selected is adequate.

The Input Amplifier amplifies the difference voltage between the inner probe points. It features very high common mode rejection (the ability to amplify only the difference voltage between the inputs and ignore any voltage which is common to both inputs) and very low input current, and stable gain. It also incorporates a zero sense and hold amplifier which eliminates input zero drift by allowing the amplifier to be zeroed prior to each measurement.

The Integrator and Zero Cross Detector is the analog portion of the analog to digital converter which is of the dual ramp type. The circuit consists of the integrator, the input selection switches (solid state) and the zero cross detector which outputs a logic signal when the integrator output has crossed zero.

The ADC Control Logic controls the integrator input selection switches,

the ADC Counter, the ADC Clock Generator based on information it receives from the zero cross detector, the ADC Clock Generator and the State Counter and Control.

The ADC Counter defines the reference period, counts the ADC clock during ramp in, stores the resulting final count and multiplexes the stored count for transmission to the display. It also provides blanking information to limit the display resolution to the range of .5 to .05% of reading.

The ADC Clock Generator supplies the clock frequencies required by the ADC Counter and Control. During the ramp-out period this frequency is 100 KHz. During ramp-in the frequency is multiplied by a constant as required by the selected measurement mode and also by the front panel multiplier in the slice resistivity or thickness measurement modes.

The Cycle Start Command Logic generates the command to start a cycle. A cycle is initiated each time the Probe Down switch is closed and also if the Retest or Reverse switches are closed providing that the Probe Down switch is still closed and that the results of the last measurement have been displayed for at least one second.

The Decimal Point and Units Select Logic selects the proper decimal point position and the proper multiplier (mΩ, Ω, KΩ, KÅ) based on information it receives from the mode switches, the message switch, the State Counter and Control, and the Range Counter and Control.

The State Counter and Control steps the FPP-100 through the proper sequence of operations. It provides the control signals for the Probe Switch Network relays and other analog and digital circuits. It receives a start command from the Cycle Start Command Logic and status signals from various analog and digital circuits as required.

The Type Circuit consists of an active filter and buffer to extract the dc component of the voltage on the third probe during the rectification type test, two comparators (N and P) to determine the polarity of the above voltage if it is greater or equal to the required magnitude, and several solid state switches which alternately connect the comparators to the output of the Input Amplifier to determine type by means of the thermally induced Seebeck voltage.

The Type Logic strobes the outputs of the N and P comparators at the conclusion of the rectification type period and stores the result. If the result of the rectification test was neither N nor P the outputs of the comparators are again strobed after they have been connected to the input amplifier in order to determine whether the type can be determined from the Seebeck voltage. If the result of the thermo-type test is still neither N nor P the Type Logic provides a pulsing signal on both the N and P output signal lines as an indication that the type could not be determined.

The Power Supply supplies the various voltages required by the FPP-100 analog and digital circuitry. It provides a logic ground output which is tied to chassis and an analog ground which is placed at the midpoint of the +14.5 volt logic supply. Thus the analog circuitry is

effectively supplied +7.25 and -7.25 volt power. It also supplies penetrate, type, display, and test current power as well as a 60V power source for the Input amplifier.

5.4 STATE CONTROL. The FPP-100 has 16 internal states which are defined and controlled by the State Counter and Control. During a measurement cycle the machine moves through the 16 states in sequence. The State Counter and Control also controls the time spent in each state and the action taken during that state. Figure 5.2 lists the states of the state counter, the action taken during each state and the condition required to leave each state.

Coincident with the turn on of power to the FPP-100 a Master Reset signal is generated which drives the state counter to the "0" state also called the Reset state. This assures that the FPP-100 comes on in a defined state. The state counter exits the Reset state and enters the Thermo-type Strobe state 2 msec after the Master Reset signal disappears. At the leading edge of the Thermo-type Strobe state the outputs of the type comparators are strobed and stored if a type test was called for. This will never be the case immediately after a Master Reset unless the type button was depressed at the same time the unit was turned on.

The Thermo-type Strobe state lasts 1 msec after which the state counter steps to the Display state. This is the normal state of the FPP-100. During the Display state the display is lighted, and all input relays are open. The display is only lighted during the Display state.

STATE NUMBER	STATE NAME	NORMAL RELAY	REVERSE RELAY	PENETRATE RELAY	TYPE RELAY	I_x RELAY	EST V_x = 5mv	EST V_x = 10mv	RAMP INTEGRATOR	ZERO	RECT TYPE STROBE	THERMO TYPE STROBE	BLANK DISPLAY	PROBE UP ABORT ENABLE	CLOCK ENABLE COMMAND CONDITION NECESSARY TO EXIT STATE
0	RESET	OPEN	CLOSE	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	NO	YES	NO	2 M SEC DELAY
1	THERMO TYPE STROBE	OPEN	CLOSE	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	EDGE	YES	NO	GAP
2	DISPLAY	OPEN	OPEN	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	NO	NO	NO	START CYCLE COMMAND
3	START DELAY	OPEN	OPEN	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	NO	YES	NO	128 M SEC DELAY
4	GAP	OPEN	OPEN	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	NO	YES	YES	GAP
5	PENETRATE	OPEN	OPEN	PEN SW CLOSED	OPEN	OPEN	NO	NO	NO	NO	NO	NO	YES	YES	4 M SEC DELAY
6	GAP	OPEN	OPEN	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	NO	YES	YES	GAP
7	ZERO	$\overline{\text{REVERSE}}$ = CLOSE	REVERSE = CLOSE	OPEN	OPEN	OPEN	NO	NO	NO	YES	NO	NO	YES	YES	(128M SEC DELAY) ($\overline{\text{CAL}}$)
8	ESTABLISH V_x			OPEN	OPEN	CLOSE	THK = 5mv	$\overline{\text{THK}}$ = 10mv	NO	NO	NO	NO	YES	YES	64 M SEC DELAY
9	ESTABLISH SHUNT			OPEN	OPEN	CLOSE			NO	NO	NO	NO	YES	YES	RANGE ACHIEVED
10	GAP			OPEN	OPEN	CLOSE			NO	NO	NO	NO	YES	YES	GAP
11	FIRST CONVERSION			OPEN	OPEN	CLOSE			YES	NO	NO	NO	YES	YES	FIRST CONVERSION COMPLETE
12	SECOND CONVERSION			OPEN	OPEN	CLOSE			YES	NO	NO	NO	YES	YES	SECOND CONVERSION COMPLETE
13	GAP	OPEN	OPEN	OPEN	OPEN	CLOSE	NO	NO	NO	NO	NO	NO	YES	YES	GAP
14	TYPE POWER	OPEN	OPEN	OPEN	TYPE SW CLOSED	CLOSE	NO	NO	NO	NO	NO	NO	YES	YES	(256M SEC DELAY) (TYPE)
15	RECT TYPE STROBE	OPEN	OPEN	OPEN	OPEN	CLOSE	NO	NO	NO	NO	EDGE	NO	YES	YES	GAP

FIGURE 5.2 STATE DIAGRAM

Exit from the Display state is inhibited until a Start Cycle Command is received at which time the state counter steps to the Start Delay state. The Start Delay state lasts for 128 msec to allow the probe to stabilize after which the state counter steps through a Gap state and into the Penetrate state. Gap states last 1 msec and are fill-in states or anti-race states which assure that a previously closed relay has time to open before another relay closes.

The Penetrate state lasts for 4 msec and the penetrate relay is closed during this time if a penetrate was called for. Following the Penetrate state the state counter steps through another Gap state into the Zero state. Upon entering the Zero state either the normal or reverse input reed relay is closed. If the last Start Cycle Command was the result of depression of the Reverse test button the reverse relay will close otherwise the normal relay will close. The Zero state also results in a Zero Command signal which activates the auto zero circuitry in both the Input Amplifier and the Current Sense amplifier and drives their outputs to zero. The zero state lasts for 128 msec unless the internal Cal switch is in the Cal position in which case the FPP-100 is inhibited from leaving the zero state until the Cal switch is taken out of the Cal position. The Cal switch is used during calibration to help in setting the auto zero set point. From the zero state the state counter steps into the Establish V_x state. In this state the I_x reed relay is closed and a signal is sent to the Current Source circuitry asking for the test current, I_x, to be increased until the inner probe voltage, V_x, reaches 5 mV in the Thickness measurement mode or 10 mV in all other modes. This state lasts for 64 msec.

After the Establish V_x state the state counter steps into the Establish Shunt state and transmits a Range Enable signal to the Range Counter and Control. The State Counter and Control remains in the Establish Shunt state until it receives a Range Achieved signal from the Range Counter and Control at which time it steps through a Gap state into the First Conversion state, state 11.

The State Counter and Control stays in the First Conversion state until it receives a First Conversion Complete signal. It then steps into the Second Conversion state. If the result of the first conversion was within range, a Second Conversion Complete is generated by the ADC Control Logic at the beginning of the Second Conversion state which results in the State Counter and Control staying only 1 msec in this state effectively skipping the second conversion. If the results of the first conversion were not within range the ADC Control Logic does not generate a Second Conversion Complete signal until the ADC has completed a second conversion at which time the State Counter and Control exits the Second Conversion state, steps through a Gap state and enters the Type Power state.

If a Type test is called for the State Counter and Control sends a signal to close the Type Power relay and remains in this state for 256 msec.

After applying Type Power for 256 msec the State Counter exits the Type Power state and enters the Rectification Type Strobe state. Coincident with entry into this state which lasts 1 msec a strobe

signal is sent to the Type Logic which stores the status of the N and P comparators whose inputs were connected to the output of the Rectification Type Buffer Amplifier throughout the Type Power state. Following the Rectification Type Strobe the State Counter and Control steps back into the Reset state, state 0. During this state which lasts 2 msec, the N and P comparators are connected to the output of the Input Amplifier which is connected to the test wafer by means of the reverse relay and is amplifying any Seebeck voltage which may exist. Upon leaving the Reset state the State Counter and Control enters the Thermo-type strobe state and transmits a strobe signal to the Type Logic which strobes and stores the state of the N and P comparators again if the result of the Rectification Type Strobe was inconclusive.

The Thermo-type Strobe state lasts 1 msec at which time the State Counter and Control steps into the Display state where it remains until it receives another Start Cycle Command signal.

5.5 ESTABLISHMENT OF THE TEST CURRENT. The FPP-100 utilizes a continuously variable test current rather than a limited number of fixed test currents as is the case in most four point probes.

The advantage of this technique is that it allows an optimum compromise between minimizing test current which is desirable (excessive test current can cause shortened probe life and errors due to sample heating and carrier injection) and maximizing the inner probe voltage signal level which is also desirable in terms of minimizing the effect of extraneous and internal error sources.

The test current is supplied by the Current Source circuit which consists of an integrating error amplifier and a logarithmic voltage to current converter. A signal from the State Counter and Control logic closes a solid state switch which connects a reference voltage and the output of the Input Amplifier through appropriate scaling resistors to the input of the integrating error amplifier. The output of the error amplifier subsequently ramps up resulting in a logarithmic increase in test current until the output of the Input amplifier reaches a level indicating an input of 10 mV (5mV in the Thickness measurement mode). The test current is then maintained at this level throughout the measurement period.

The current source is capable of supplying any current between 400 na and 400 ma. The maximum output current is limited at between 400 and 500 ma in order to avoid excessive currents.

The maximum output voltage of the current source is approximately 40 volts for test currents less than 400 na which means that for high resistivity samples the FPP-100 can tolerate a contact resistance of greater than 2,000 times the sample V/I before the current source compliance limit is reached. Even if the desired test current cannot be established (because of excessively high contact resistance or because of intentional current limiting) the resulting measurement will not be seriously in error because the FPP-100 performs a true measurement.

The compliance voltage of the FPP-100 is intentionally reduced as the

test current is increased in order to limit the maximum power that can be dissipated in the test sample.

Figure 5.3 shows the FPP-100 test current as a function of V/I, and maximum compliance voltage of the FPP-100 as a function of V/I.

5.6 ESTABLISHMENT OF RANGE. After the test current has been established the range of the Current Sense circuit must be established. The Current Sense circuit has 6 ranges each separated by one decade. The minimum voltage transfer coefficient (effective shunt value) is 8.825Ω which results in an output voltage of 4.0 volts at an input sheet resistivity of 0.1 Ω/sq. and a test current of 453 ma. As the test sample sheet resistivity increases the test current drops. In order to keep the Current Sense circuit output within an acceptable level the value of the effective transfer resistance is increased by a factor of 10 every 64 msec until the output level is greater than 425 mV or until the final range has been reached. A comparator on the output of the current sense amplifier produces a Range OK signal if the output of the amplifier is above 425 mV. This signal indicates to the Range Counter and Control that the Current Sense Range is adequate and a Range Achieved signal is sent to the State Counter and Control resulting in termination of the Establish Range state.

5.7 RESISTIVITY MEASUREMENT. Once the test current and the current sense circuit range have been established the basic sheet resistivity measurement is accomplished by means of the Integrator and Zero Cross Detector, the ADC Counter and Control, and the ADC Control logic

operating in conjunction with the ADC Clock Generator.

The analog to digital converter in the FPP-100 is of the dual ramp type. In this type of converter one input is connected to an integrator for a fixed amount of time during which time the integrator output ramps-out (away from zero). Immediately following the fixed ramp-out time the second input is applied to the integrator with reversed polarity so that the integrator output ramps in (toward zero). The time it takes for the integrator output to ramp back to zero is equal to the ratio of the first input to the second input multiplied by the reference ramp-out time. If the ramp-in time is used to gate a pulse train into a counter the resulting number accumulated in the counter will be directly related to the ratio of the two inputs.

In the FPP-100 the ramp-out time is fixed at 100 msec. This time corresponds to an integral number of line voltage cycles at both 50 Hz and 60 Hz which results in minimum susceptibility of the FPP-100 to noise or ripple at line frequency or multiples thereof.

For sheet resistivity, slice resistivity, and V/I measurements the integrator ramps-out on V_{xa} (the amplified inner probe voltage) and ramps-in on V_{sa} (the amplified current sense voltage) so that the count time is directly proportional to the ratio V/I. To make the output count equal to sheet resistivity, slice resistivity or V/I the counter clock (pulse train) frequency is modified to include the proper proportionality constant and in the case of slice resistivity to include the front panel thickness constant.

Figure 5.4 lists the clock frequencies used.

In the thickness measurement mode the integrator ramps-out on V_{sa} and in on V_{xa} thus the count period is proportional to I/V. For a film with defined bulk resistivity the thickness is proportional to I/V thus selection of the proper clock frequency, which includes the front panel bulk resistivity multiplier, results in a displayed number equal to the film thickness in KÅ.

When a sheet resistivity, slice resistivity, or V/I measurement is made, the polarity of the voltages in the FPP-100 in such that the integrator ramps positive during the integration of V_{xa} and then back to zero during the integration of V_{sa}. (When a Thickness measurement is made the integrator output ramps negative on V_{sa} and then back to zero on V_{xa}).

The integrator output is clamped at zero, except during a conversion, by a solid state switch refered to as the Dump switch. In order to assure that the output state of the zero cross detector is known prior to the start of ramp-out, the reference to the zero cross comparator is biased up to +10mV for Sheet, Slice and V/I measurements and biased down to -10 mv for Thickness measurements.

Inputs very close to zero can result in a very long delay before the integrator output crosses the zero detector threshold.

If the time to cross zero exceeds 1024 msec the ADC Control Logic assumes the input is negligibly close to zero and generates a Master

V/I	TEST CURRENT	MAXIMUM COMPLIANCE VOLTAGE
1 mΩ	.5A Max	7V
10 mΩ	.5A Max	7V
20 mΩ	.5A	7V
100 mΩ	100 mA	15V
1Ω	10 mA	18V
10Ω	1 mA	40V
100Ω	100 µA	45V
1000Ω	10 µA	48V
10KΩ	1 µA	50V
40KΩ	250 NANOA	50V

FIGURE 5.3 TEST CURRENT AND COMPLIANCE VOLTAGE AS A FUNCTION OF V/I.

MODE	MESSAGE MULTIPLIER	ADC CLOCK FREQUENCY
Sheet	Geo. Corr. All Others	200 KHZ (M) 200 KHZ
Slice	x 1 Mil x 10 Mil x 1µ x 10µ x 100µ	50.8 KHZ (M) 50.8 KHZ (M) 200 KHZ (M) 200 KHZ (M) 200 KHZ (M)
Thickness	x 1µ Ω cm x 10µ Ω cm x 100µ Ω cm	50 KHZ (M) 50 KHZ (M) 50 KHZ (M)
V/I	Geo. Corr. All Others	44.1 KHZ (M) 44.1 KHZ

FIGURE 5.4

Reset signal which returns the FPP-100 to the display state and results in a display of zero.

Very large inputs can result in a very long time required to ramp back in to zero. If this time exceeds 924 msec the ADC Control Logic signals an overrange condition by generating a signal which forces a display of overrange and 999, and by driving the FPP-100 to the Display state by means of a Master Reset.

5.8 PENETRATION FUNCTION. If selected, the penetration function applies a high voltage low energy pulse to the probe points prior to the resistivity and type tests. This pulse occurs immediately after the 128 msec start delay and is accomplished by closing a 4 pole reed relay for 4 msec. One probe pin is connected to ground while the other three are connected to a +170V dc supply through individual 10 MΩ resistors. The maximum energy dissipated at the probe points is 30 watt-sec.

The penetrate function can be internally disabled by a switch accessible by removing the bottom calibration access cover.

5.9 TYPING FUNCTION. Two different methods are commonly used to determine the semiconductor type of a test wafer. The first of these methods is referred to as the rectification method. This method relies on achieving rectifying junctions at the probe contact point. In this method three contacts to the wafer are used, one is grounded and an AC voltage is applied to the second. The third contact is used to monitor the voltage developed on the wafer. Negligible

current is drawn through the third contact so that the nature of this contact junction is not critical.

If the probe contacts are partially rectifying, a dc voltage will be developed on the wafer in addition to any ac voltage which is present. A negative dc voltage indicates P type material a positive dc voltage indicates N type material. The success of this method depends on the ability to achieve rectifying junctions which is a function of surface preparation, probe point pressure and probe point condition and becomes increasingly difficult as the sample resistivity decreases.

The second method of determining semiconductor type is refered to as the thermoelectric effect and utilizes the polarity of the Seebeck voltage produced by a thermal gradient in the material.

The thermoelectric effect is most easily used on low resistivity materials and indeed can give erroneous results when used on high resistivity materials where carrier mobility becomes important.

Fortunately the application ranges for the two typing methods described above overlap so that the material type can generally be determined by one of the two methods.

In performing a type test the FPP-100 first looks for a rectification effect. One probe pin is grounded while 14 VAC is applied to a second. The dc potential of the wafer, if any, is monitored by a third probe pin. The 14 VAC power is applied for 256 msec at the end of which time the average dc voltage on the third probe pin is sampled.

If this voltage is greater than 0.5 VDC the polarity is used to determine the displayed material type.

Immediately after removing the type power the FPP-100 connects the Input amplifier to the third probe pin and one of the probes pins through which the type power was applied. In general there will be a thermal gradient between these probe contact points because of local heating in the material at the type power contact. Any Seebeck voltage resulting from this thermal gradient is monitored by the Input amplifier. If the magnitude of this voltage is greater than 0.5 mVDC the material type is determined from the polarity providing that the results of the rectification test were inconclusive.

If the magnitude of the Seebeck voltage is less than 0.5 mVDC and the results of the rectification test were inconclusive the FPP-100 indicates an inconclusive type test by flashing the N and P indicators.

The amount of power dissipated at the type power probe points depends on the contact resistance and reaches a maximum value of approximately 2.7 watts when the sum of the contact resistances is equal to 18Ω. The maximum amount of energy that can be supplied to the wafer (approximately 0.7 joules) would result in a temperature rise of less than 0.5°C if supplied evenly to a typical two inch wafer.

The type function can be internally disabled by means of a switch reached by removing the access plate on the bottom of the FPP-100.

SECTION 6

CIRCUIT DESCRIPTION

6.0 INTRODUCTION. This section describes the circuits of the FPP-100. Power Supply Schematic Figure 8.1 shows the inter-relationship between the different circuits in the unit.

6.1 POWER SUPPLY BOARD. See Power Supply Schematic Figure 8.1 for details. These voltages are the main power of +14.5V, the signal ground reference of +7.25V, the display power of +5V, the type power of 14VAC, and the input amp power of +60V. It also supplies the probe power, and the +170V penetrate power voltage.

6.2 ANALOG BOARD REF. FIG. 8.6. This board contains the probe switching relays, input amplifier, current source, current sensing, analog to digital converter, type, and comparator voltage divider circuitry.

6.2.1 PROBE SWITCHING RELAYS. The switching relays, K1 through K5, connects the probe head to the various sections of the analog board depending on the mode of operation. Shown in Table 6.1 is the relay switching logic as a function of the FPP-100 system states.

6.2.1.1 PENETRATE RELAY K1. Relay K1 connects the penetrate power of 170V through resistors R27 through 29 to the probe head whenever

the penetrate mode is activated.

6.2.1.2 TYPE RELAY K2. Relay K2 connects the typing circuitry to the probe head whenever the typing mode is activated.

6.2.1.3 NORMAL RELAY K3 AND REVERSE RELAY K4. Relay K3 connects the current source, current sense circuitry, and input amplifier to the probe head when the system is measuring any function of V_x/I_x or thickness in the NORMAL mode. Relay K4 performs the same function in the REVERSE mode.

During the AUTO ZERO state relays K3 and K4 are activated simultaneously to short the input to the input amplifier. Relay K4 is also used during the Thermo-type mode to connect the input amplifier to the probe head.

6.2.1.4 I_x RELAY K5. Relay K5 connects the current source through the contacts of either relay K3 or K4 to the probe head when the system is measuring any function of V_x/I_x or thickness. As shown in Table 6.1 Relay K5 is open during system states 0 through 7 and is closed during system states 8 through 15.

6.2.2 INPUT AMPLIFIER. The input amplifier is made up of two high input impedance FET input operational amplifiers, Z1 and Z2, whose supply voltages are bootstrapped to the common mode signal to improve the CMRR of the input amplifier. The supply voltage for Z1 and Z2 are floating supplies with the upper supply rail provided by constant current source Q1, resistors R5 and R6, and emitter follower Q3. The

lower supply rail is provided by constant current source Q7, resistors R8 and R10, and emitter follower Q6.

Constant current source Q2 provides the bias currents through gain setting resistors R3 and R4. With a zero differential signal to the input amplifier the bias currents through R3 and R4 are equal. Otherwise, any differential input signal, V_x', to the input amplifier will result in a differential voltage across the R3 and R4. This differential voltage will create a differential current, Δi, through transistors Q4 and Q5.

$$\Delta i = \frac{V_x'}{R_3 + R_4}$$

If R18 is equal to R19, and R12 is equal to the parallel combination of R16 and R17, the input amplifier output voltage, V_x, is

$$V_x = 2R_{12}\, i$$

Thus, the input amplifier gain is

$$G_x = \frac{V_x}{V_x} = \frac{2R_{12}}{R_3 + R_4} = \frac{2\ (10K)}{2\ (49.9)} = 200.4\ V/V$$

The input amplifier offset drifts are canceled out by the auto zero circuit. During system state 7, the inputs to the input amplifier are shorted together through the relay contacts of K3 and K4. Sample and hold amplifier Z4, with switch Z11C closed, will drive V_x to zero to cancel the input amplifier offset voltage drifts. For all other systems states, switch Z11C is opened and the offset correction voltage is held by Z4.

Resistor R9 is used to set the coarse offset adjustment in the input amplifier. Resistor R21 is used to set the zero reference for Z4.

SYSTEM STATE	MODE	PENETRATE RELAY K1	TYPE RELAY K2	NORMAL RELAY K3	REVERSE RELAY K4	I_X RELAY K5
0	Reset	Off	Off	Off	On	Off
1	Thermo-strobe	Off	Off	Off	On	Off
2	Display	Off	Off	Off	Off	Off
3	Start Delay	Off	Off	Off	Off	Off
4	Gap	Off	Off	Off	Off	Off
5	Penetrate	Pss	Off	Off	Off	Off
6	Gap	Off	Off	Off	Off	Off
7	Zero	Off	Off	$\overline{R}$	R	Off
8	Establish V_x	Off	Off	$\overline{R}$	R	On
9	Establish Shunt	Off	Off	$\overline{R}$	R	On
10	Gap	Off	Off	$\overline{R}$	R	On
11	Ramp 1	Off	Off	$\overline{R}$	R	On
12	Ramp 2	Off	Off	$\overline{R}$	R	On
13	Gap	Off	Off	Off	Off	On
14	Rect Type	Off	Tss	Off	Off	On
15	Rect Strobe	Off	Off	Off	Off	On

Tss = Type Switch Stored
Pss = Penetrate Switch Stored
R = Reverse Switch
$\overline{R}$ = Not Reverse Switch

TABLE 6.1 SUMMARY OF PROBE SWITCHING RELAY OPERATION.

6.2.3 CURRENT SOURCE. The current hold loop maintains a constant voltage V_x' across the inner probe leads when the current hold loop is activated. This voltage is either 5 mV or 10 mV, depending on the logic command signals to switches Z16A and Z16B. When the current hold loop is activated, integrator Z10 will compare the reference voltage with the integrator voltage up to drive the log current source (transistor network Q13 through Q16). The current source gain is an approximate logarithmic function to maintain an approximate constant loop gain at all probe current values in the current hold loop.

The current hold loop will supply the current, I_x, to the probes to hold the voltage across the inner probes to the reference setting (either 5 mV or 10 mV). For test samples with very low resistivity values,

the clamp circuit (R37, R38, and CR6) will clamp the current source to a maximum current of approximately 1/2 amp.

6.2.4 CURRENT SENSE AND RANGE ACHIEVED DETECTOR. The current sense circuitry senses the probe current, I_x and converts this current to an output voltage V_x, proportional to probe current. The probe current passes through one of three possible legs of the current shunt, and generates a voltage, V_s', proportional to probe current.

$$V_s' = I_x R_{shunt}$$

V_s' is amplified by the current shunt amplifier, Z8. The current shunt together with the current sense amp generates the necessary gain for the selected range. The gain is controlled by the logic signals sw1, sw2, sw3, swA, and swB which are controlled by the automatic ranging circuitry discussed in Section 6.3.3. Shown in Table 6.2 are the values of nominal shunt resistance and current sense amplifier gain for each of the six decade ranges of the current sense circuitry. Pots R59, R62, R67, and R70 are used to adjust the current sense gains during system calibration.

The range achieve detector Z6D, is used in the automatic ranging mechanization to detect when the current sense range has been achieved. Detector, Z6D, output goes true when the current sense output voltage, V_s, greater than 425 mV.

RANGE	SW1	SW2	SW3	SWA	SWB	NOMINAL R_{SHUNT} (Ω)	NOMINAL GAIN K_S (V/I)
1	T	F	F	T	F	2	4.413
2	T	F	F	F	T	2	44.13
3	F	T	F	T	F	200	4.413
4	F	T	F	F	T	200	44.13
5	F	F	T	T	F	20K	4.413
6	F	F	T	F	T	20K	44.13

TABLE 6.2 SUMMARY OF CURRENT SHUNT OPERATION.

6.2.5 INTEGRATOR AND ZERO CROSS DETECTOR. The analog to digital converter (A/D) utilizes the double ramp concept described in Section 5.3 to convert the ratio of V_X/V_S or V_S/V_X into a digital number. For the V/I, bulk and sheet measurements, the integrator Z7 is ramped up by switching in V_X (a negative voltage) through switch Z13D. The integrator is ramped down by opening switches Z13D and closing switch Z13B to switch V_S (a positive voltage). For THK measurements the switching procedure is reversed to ramp the integrator output down and then back up. Switch Z15D shorts the integrator capacitor, C12, when the ADC is not in the conversion mode. Pot R75 is used to null the integrator offset voltage during calibration.

The zero cross detector, Z6B, changes logic state whenever the integrator output crosses its reference voltage. The reference voltage is +10 mV for the V/I, bulk and sheet measurements and -10 mV for the THK measurements.

6.2.6 TYPE CIRCUIT. The type circuit types the material under test if the type test is desired. As discussed in Section 5.3 if a type test is selected, a rectification test is tried first. If the results

are inconclusive a thermo-type test is attempted. As shown in Figure 8.6 rectification test type power is applied to probe tips 1 and 2. The rectification signal on probe tip 3 is switched to a low pass filter whose output is buffered with the unity gain amplifier, Z5, and filtered through another low pass filter stage (R44 and C10). The filtered rectification voltage is then applied to the typing comparators Z6C and Z6A. If the filtered rectification voltage is greater than +93 mV the N type comparator, Z6C, will go true. If the filtered rectification voltage is more negative than -93 mV, the P type comparator, Z6A, will go true.

If the absolute value of the filtered rectification voltage is less than 93 mV, the material type cannot be determined by the rectification type test and the system will be switched to the thermo-type test. The thermoelectric voltage across probe tips 2 and 3 will be switched through the reverse relay (K4) and amplified by the input amplifier with a gain of 200.4. The amplified thermoelectric voltage is switched through switch Z16C to the low pass filter (R45 and C10) and type comparators. Again, if the absolute value of the amplified thermoelectric voltage is greater than 93 mV, the material can be typed as described above for the rectification test. Otherwise, the thermo-type test results are inconclusive.

6.2.7 COMPARATOR VOLTAGE DIVIDER. This voltage divider consisting of resistors R48 through 54 provides the voltage references for the type circuit, A/D zero cross, and current sense range achieve comparators.

6.3 STATE COUNTER AND CONTROLS REF. FIGURE 8.5. The State Counter and Control consists of a 4 bit, fully decoded mod 16 binary counter. The basic clock is a 1 KHZ and is enabled as a function of the clock enable command. Z27 is the 4 bit binary counter. Z28 and Z21 decode the 16 states, and Z15 and Z8 enable the clock as a function of input information. Z14 is considered the Timer, and has a basic clock of 1 KHZ. The Timer is reset to zero on every change of the State Counter.

6.3.1 STATE COUNTER AND CONTROL INPUTS, REF. FIGURE 6.1 AND 8.5. The basic inputs to the State Counter and Control section are the functions necessary to enable the State Counter Clock. Z15 and Z8 are configured into a single 16 channel multiplexer. Pin 3 on Z15 and Z8 is the output of the multiplexer. When pin 3 is a logic zero the clock is not enabled and the state counter will not advance. The 16 inputs to the multiplexer are time delays from the Timer, Cycle Start Command, Range Achieved, and Control Function for Analog to Digital Conversions, as indicated on the state control diagram. The start cycle command is generated as a function of data stored in the quad latch Z16. If the unit is in the display state and the probe goes down, the State Counter clock will be enabled and the cycle will commence. If the probe is down and retest or reverse current is depressed the cycle will commence. A cycle cannot start if the probe is not down.

6.3.2 STATE COUNTER AND CONTROL OUTPUTS, REF. FIGURE 6.1 AND 8.5. The outputs of the State Counter and Control consist of the 4 bit binary output of the State Counter Z27 pins 3, 4, 5, and 6, and the

STATE NUMBER	STATE NAME	K3 NORMAL RELAY	K4 REVERSE RELAY	K1 PENETRATE RELAY	K2 TYPE RELAY	K5 I_X RELAY	EST V_X = 5mv	EST V_X = 10mv	RAMP INTEGRATOR	ZERO	RECT TYPE STROBE	THERMO TYPE STROBE	BLANK DISPLAY	PROBE UP ABORT ENABLE	CLOCK ENABLE COMMAND CONDITION NECESSARY TO EXIT STATE
0	RESET	OPEN	CLOSE	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	NO	YES	NO	2 M SEC DELAY
1	THERMO TYPE STROBE	OPEN	CLOSE	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	EDGE	YES	NO	GAP
2	DISPLAY	OPEN	OPEN	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	NO	NO	NO	START CYCLE COMMAND
3	START DELAY	OPEN	OPEN	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	NO	YES	NO	128 M SEC DELAY
4	GAP	OPEN	OPEN	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	NO	YES	YES	GAP
5	PENETRATE	OPEN	OPEN	PEN SW CLOSED	OPEN	OPEN	NO	NO	NO	NO	NO	NO	YES	YES	4 M SEC DELAY
6	GAP	OPEN	OPEN	OPEN	OPEN	OPEN	NO	NO	NO	NO	NO	NO	YES	YES	GAP
7	ZERO	$\overline{\text{REVERSE}}$ = CLOSE	REVERSE = CLOSE	OPEN	OPEN	OPEN	NO	NO	NO	YES	NO	NO	YES	YES	(128M SEC DELAY)($\overline{\text{CAL}}$)
8	ESTABLISH V_X			OPEN	OPEN	CLOSE	THK = 5mv	$\overline{\text{THK}}$ = 10mv	NO	NO	NO	NO	YES	YES	64 M SEC DELAY
9	ESTABLISH SHUNT			OPEN	OPEN	CLOSE			NO	NO	NO	NO	YES	YES	RANGE ACHIEVED
10	GAP			OPEN	OPEN	CLOSE			NO	NO	NO	NO	YES	YES	GAP
11	FIRST CONVERSION			OPEN	OPEN	CLOSE			YES	NO	NO	NO	YES	YES	FIRST CONVERSION COMPLETE
12	SECOND CONVERSION			OPEN	OPEN	CLOSE			YES	NO	NO	NO	YES	YES	SECOND CONVERSION COMPLETE
13	GAP	OPEN	OPEN	OPEN	OPEN	CLOSE	NO	NO	NO	NO	NO	NO	YES	YES	GAP
14	TYPE POWER	OPEN	OPEN	OPEN	TYPE SW CLOSED	CLOSE	NO	NO	NO	NO	NO	NO	YES	YES	(256M SEC DELAY)(TYPE)
15	RECT TYPE STROBE	OPEN	OPEN	OPEN	OPEN	CLOSE	NO	NO	NO	NO	EDGE	NO	YES	YES	GAP

FIGURE 6.1 STATE DIAGRAM

16 decoded states from Z28 and Z21. The 4 bit binary output of Z27 is also used to address the 16 channel multiplexer Z15 and Z8. General decoding of the State Counter and input switches determine the configuration of the probe network along with addressing the solid state switches on the analog board.

6.3.3 RANGE COUNTER AND CONTROL REF. FIGURE 8.5. The Range Counter and Control consists of a resettable 3 bit binary counter Z27 pins 11, 12, 13, with a gated clock. The range counter is reset to zero during State 3. The clock to the Range Counter is inhibited until State 9 (Establish shunt). The Range Counter clock will occur once every 64 milliseconds. The clock is enabled during State 9 until the Range Achieve Signal occurs Or until the range counter reaches State 5. The "or" function will clear Z20 pin 13 which will inhibit the Range Counter Clock, and the unit will step to State 10.

6.3.4 ADC CLOCK GENERATOR, REF. DIGITAL I SCHEMATIC FIGURE 8.4. The Basic System Clock is a 1MHZ, crystal controlled oscillator consisting of Y1, R2, Z23, and Z29. This 1 MHZ clock is multiplied by constants and variables to generate the correct scaled count pulses for the analog to digital conversions. Z22, Z15, Z8, and associated logic make up the "C" Multiplier. The inputs to the "C" multiplier are switch functions V/I, thickness, slice, sheet, and message. The "C" multiplier is a 3 decade rate multiplier. The output of the "C" multiplier is Z8 pin 6 (TP-5). If V/I was the input selection, we multiply the basic clock (1 MHZ) by .441. The multiplier input on Z22 pins 14, 15, 2, 3, are set to 4, Z15 inputs set to 4 and Z8 inputs set to 1, thus for every 1,000 input pulses we have 441 output pulses. The output frequency

at Z8 pin 6 (TP-5) is as follows:

INPUT	OUTPUT FREQUENCY
V/I	441 KHZ
Thickness	500 KHZ
Slice x 1 Mil/10 Mil	508 KHZ
Slice x 1μ/10μ/100μ	200 KHZ
Sheet	200 KHZ

Z15 pin 1 outputs a 10 KHZ signal that is used for display conditioning. Z8 pin 1 outputs a 1 KHZ signal which is used to clock the State Counter, Timer, and scan the ADC digit drivers.

The "M" Multiplier Ref. "M" Multiplier schematic Figure 8.3, is also a 3 decade rate multiplier. The "M" Multiplier is used in conjunction with Thickness and Slice Measurements, and geometry corrections for V/I and sheet. The variable parameters of thickness, slice, and geometry correction are inputted via 3 decades of thumbwheel switches. Thus multiplying the "C" Multiplier constants by the "M" Multiplier variables.

The clock input of the "M" Multiplier is pin 9 on Z3, Z2, and Z1. This clock input is the output of the "C" Multiplier. Input clock frequencies of 508 KHZ, 500 KHZ, 441 HHZ, and 200 KHZ are multiplied by the 3 decades of thumbwheel switch information to derive the "M" Multiplier output, Z1 pin 6 (TP-1).

In this section we have discussed the basic clock, the "C" Multiplier, and the "M" Multiplier. Each of these functions will be divided by 1, 10, or 100 depending on input selection and control logic commands.

The divide change consists of Z12 (Solid State Switches), and associated control logic. The output of the divide change is connected to flip-flop Z4 pin 5 which is used as a squaring circuit to insure a proper ADC Clock duty cycle.

6.3.5 ADC CONTROL LOGIC, REF. DIGITAL 1 SCHEMATIC FIGURE 8.4. The zero cross signal from the analog board is made available to Z6 pin 2. Z6 is an Exclusive "OR" gate, and will invert the Zero Cross Signal for all measurements other than Thickness. The Zero Cross function is then synchronized and delayed via a 2 bit shift register Z27. During State 11 the 2 bit shift register Z27 is enabled. Zero Cross Sync is generated when Z27 pin 5 goes from a lgoic zero to a logic 1, followed by a rising edge clock pulse on Z27 pin 3. Zero Cross Delay is generated on the next rising edge clock. Zero Cross Sync is "anded" with $\overline{\text{Zero Cross Delayed}}$ via Z21 pins 1 and 2 to generate a reset pulse. This reset pulse resets Z9 (ADC Display Counter) to 0000. Zero Cross Sync (Z27 pin 1) being a logic 1 enables the ADC Clock to be counted by Z9 (ADC Display Counter) via gate Z11 pins 11, 12, and 13. Zero Cross Sync being a logic 1 also enables the Ramp Control Flip-Flop (Z20 pin 1) to change from ramp-out to ramp-in. The Ramp Control Flip-Flop is normally in the Ramp-Out state, (Z20 pin 1 at logic zero). This Ramp-Out state, commands an ADC Clock (during State 11 or 12) of 100 KHZ. The Extend output of the Display Counter Z9 will go from a logic zero to a logic 1 at a count of 9999. This Extend Pulse, "Anded" with Zero Cross Sync will clock the Ramp Control Flip-Flop from Ramp-Out to Ramp-In. The time from Zero Cross Sync to Ramp-In is 100 milliseconds which is the time required to count from 0000 to 9999 at a Ramp-Out clock rate of 100 KHZ (10 microseconds/count). The Ramp-Out clock

is always 100 KHZ. The Ramp-In clock will be counted by the Display Counter until Zero Cross Sync goes to a logic zero. Zero Cross Sync at a logic zero Anded with Zero Cross Delay at a logic 1 generates a Transfer Pulse via Z13 pin 10. This Transfer Pulse transfers the contents of the Display Counter into 4 decades of storage (Z9). Transfer also terminates the conversion. Z20 pin 13 is the Overrange Flip-Flop. An extended pulse during Ramp-In will generate Overrange. If we overrange during State 11 the unit will automatically convert again in State 12.

The unit will automatically "Time Out" for measurements too small or too large to convert. If after 1024 milliseconds in state 11 or 12 the conversion is not complete, Z25 pin 11 will generate a clock pulse to flip-flop (Z4 pins 12 and 13) will store the state of the Ramp Control flip-flop (Z20 pin 1). If the unit was in Ramp-Out the display will read 0000. If the unit was in Ramp-In, Z4, pin 12 will be used to invert the 1 bit and the 8 bit of the display data via Z1 pins 10 and 11, thus displaying 9999. Z4 pin 13 will set the overrange flip-flop resulting in a 9999 display and overrange.

6.3.6 ADC COUNTER AND DISPLAY CONDITIONING REF. FIGURE 8.4. Z9 is the ADC Counter. Z9 functions as a resettable 4 decade counter with 4 decades of storage. The output data is multiplexed complementary binary coded decimal (BCD), pins 10, 11, 12, and 13. The Digit Drivers are pins 1, 2, 3, and 4. Pin 4 (10°) is the LSD. The Scan Rate of the multiplexed data is controlled by the signal on Pin 9. Pin 9 is 1 KHZ, therefore, the scan rate is 250 times a second. The BCD output data is connected to Z17 (BCD to 7 segment decoder).

Z17 drives Z16 (transistors) which saturate in order to turn on the segments. The Digit Driver Circuit consists of Z10, Q1, Q2, Q3, and Q4. Q1 will saturate to +5 volts when the thousands decade is addressed by Z9. The display conditioning is controlled by the Blanking input Z17, pin 4. Z3, pin 1 conditions the MSD by decreasing the ON time of the display. Z3 pin 2 does the same for the LSD. Z3, pin 12 turns off the LSD.

6.3.7 DECIMAL POINT AND MULTIPLIER SELECTION REF. FIGURE 8.5. Decimal Point and Multiplier Selection is determined by input switch selection, thumbwheel switch message, Range Counter State, and A to D conversion state. This information is made available to a 256 by 8 bit ROM, (Z22). The ROM decodes the input information, and outputs 2, 4 bit selections (A & B). Section A is coded information dealing with a conversion in State 11. Section B is coded information dealing with a conversion in State 12. This information is made available to a Quad 2 Channel Data Selector Z9. The address for the Data Selector is generated by flip-flop Z23 pins 1 and 2, Z23 determines whether the conversion was during State 11, or State 12, thus addressing the proper 4 bit Section A or B to the output of Z9. The output data of Z9 is then decoded by Z1 and made available to the display and decimal point driver circuits.

6.3.8 TYPE LOGIC AND CONTROL. REF FIGURE 8.5. If the Type function is selected Z10 pin 9 will be set to a logic 1, turning on the type indicator, and causing the State Counter clock to be inhibited for 256 milliseconds during State 14. Flip-flops Z25 pins 5 and 9 will interrogate the N and P Comparators on the analog board. On the exit

of State 14, a rising edge clock (TP-8) will strobe flip-flops, Z25, thus interrogating N and P. If either N or P are logic 1's, Rectification Typing was successful and typing is complete. If N and P are logic zero a second strobe will be generated on the exit of state 1. If N or P are logic 1's Thermo-typing was successful. If N and P are still logic zero, Z25 pins 2 and 12 will be logic 1's and both N and P indicators will flash indicating the unit could not type.

SECTION 7

MAINTENANCE

7.1 MAINTENANCE PHILOSOPHY. The FPP-100 has been designed to minimize maintenance by the use of high quality components and field removable printed circuit boards. This section will outline the procedure for light maintenance and identifying general problem areas. It is strongly recommended that maintenance be limited to locating defective circuit boards and replacing them, removing and replacing probe heads, and general calibration. Before troubleshooting is started a troubleshooter should thoroughly read and understand Section 6. Internal photographs, see Figures 7.1, 7.2, and 7.3, together with complete schematics, Section 8., show all pin numbers and interconnections, and printed circuit board locations.

7.2 TROUBLESHOOTING. Should difficulties be encountered in the use of the FPP-100, the casting will have to be removed in order to expose the electronics.

7.2.1 CASE REMOVAL.

a. Disconnect the power cord.

b. Place the FPP-100 on its side so the unit is balancing on the cover.

c. Remove the six Mounting Screws Ref. Figure 4.1.

d. Carefully remove the chassis and place it on its rubber feet.

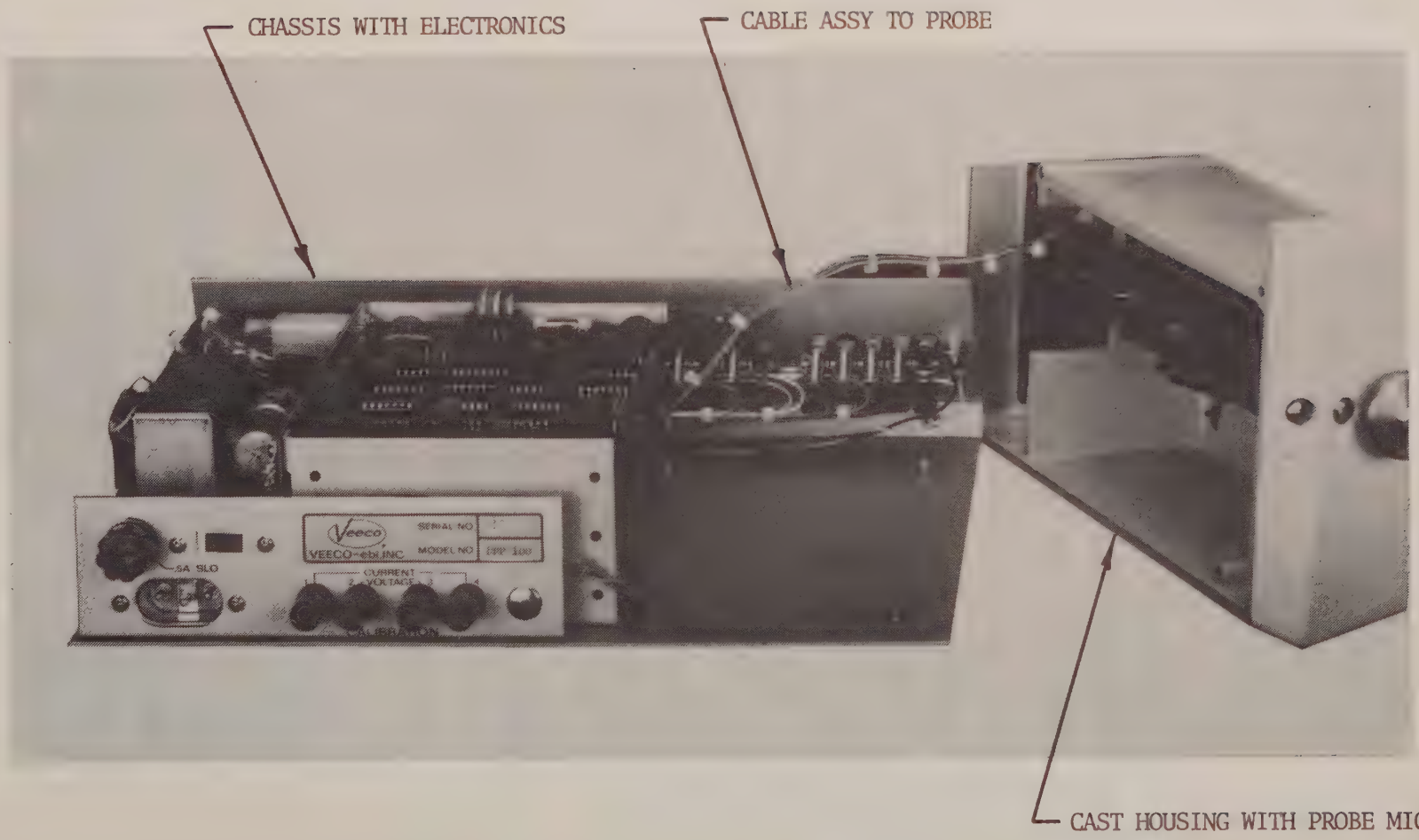


FIGURE 7.1 CASE REMOVAL

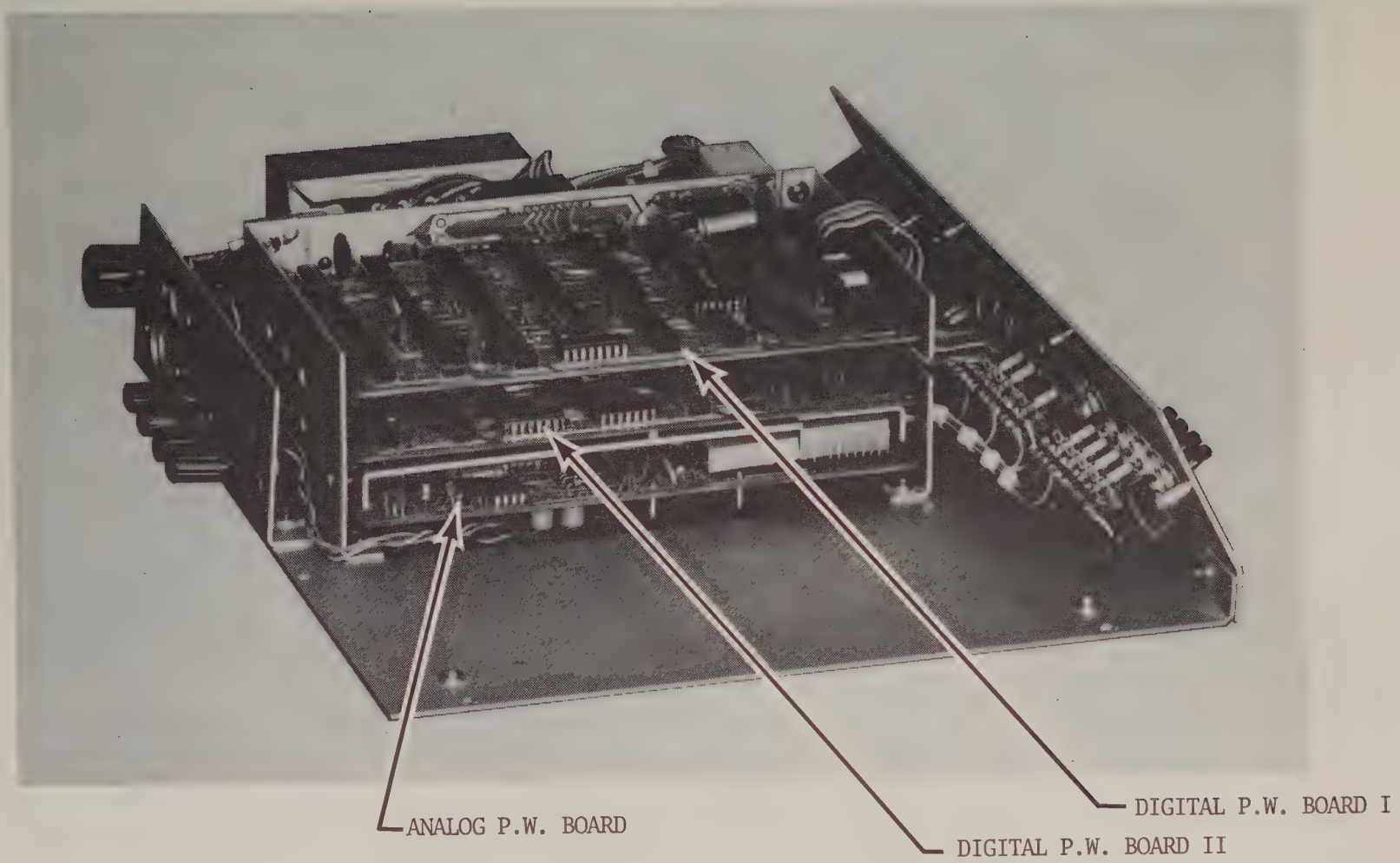


FIGURE 7.2 FPP-100 INTERIOR

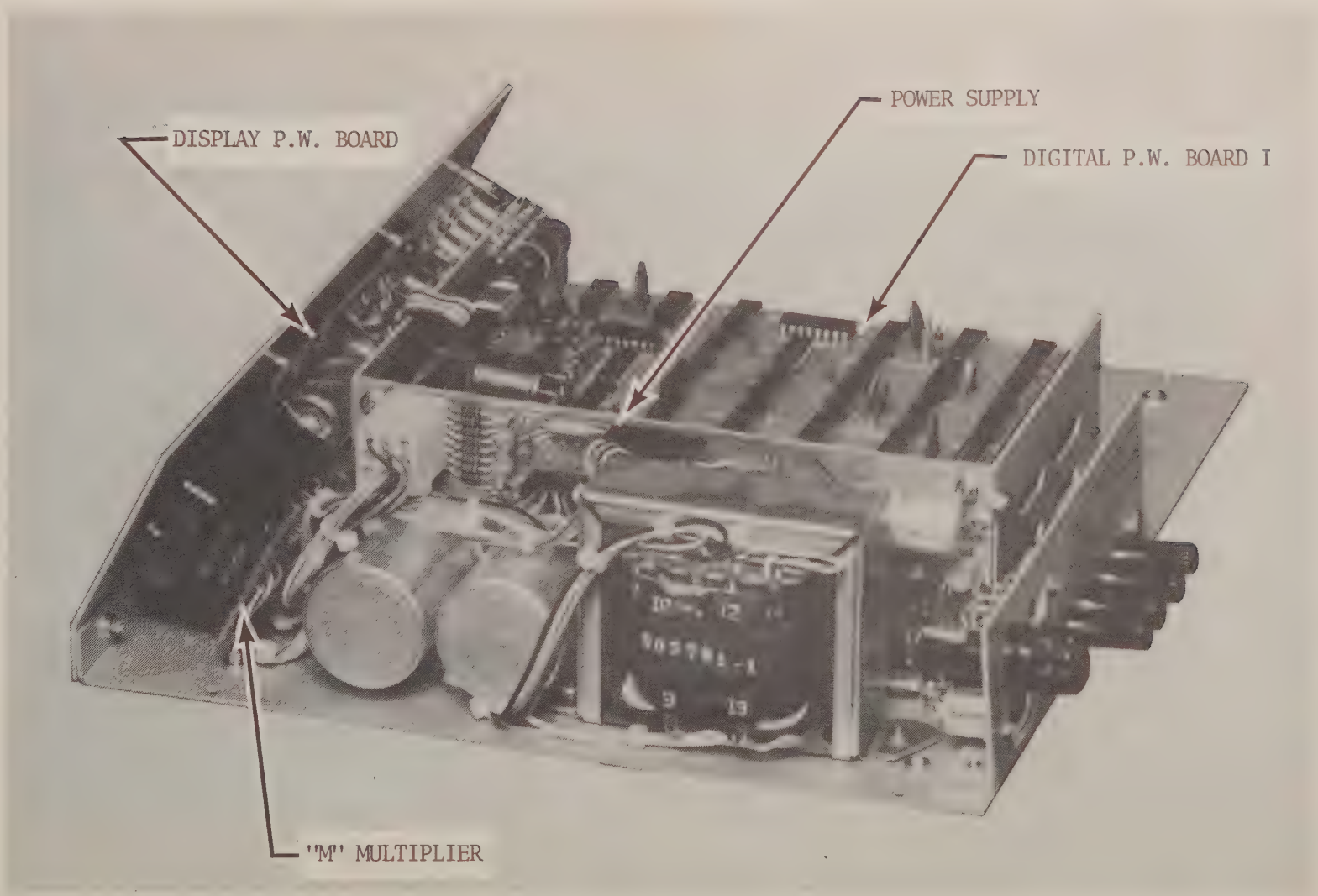


FIGURE 7.3 FPP-100 INTERIOR

WARNING: EXTREME CARE SHOULD BE TAKEN WHEN SERVICING THE FPP-100. SURFACES WITH HIGH POTENTIALS ARE EXPOSED WHEN THE CASE IS REMOVED.

7.2.2 POWER SUPPLY REF. FIGURE 8.1.

NOTE: The power supply should not be checked unloaded. All supply voltages should be measured in respect to power (chassis) GND, unless otherwise specified. The power transformer, T1, can be easily removed for accessibility to the power supply components.

a. +14.5VDC. Z2 is the +14.5 regulator. R12 is used to adjust the +14.5VDC supply to 14.5VDC ±100mv.

b. Signal GND. Z1 is used to generate signal GND. Signal GND equals +7.25VDC ± 50mv.

c. Display Power. CR4, CR5, and C4 are used to generate display voltage. Additional filtering of the display voltage is on the display board. The display voltage (loaded) is +5VDC ±20% and is unregulated.

d. Type Source Power. 14VAC direct from T1 thru current limiting resistor R1.

e. Penetrate Power. +170 volts derived from T1 pin 14. C1, CR1, CR10, and C6.

f. Probe Power. +50 volts probe power is generated via CR12 (51V Zener) and pass transistor Q2.

g. Input and Power. +60 volt input amp power is generated via CR12, CR13, (+61V) and pass transistor Q2.

7.2.3 DISPLAY AND 'M' MULTIPLIER REMOVABLE REF. FIGURE 7.2 and 7.3.

The display board and 'M' multiplier assembly are mounted to the front

panel. The top two printed circuit boards must be removed in order to detach the front panel. Once the front panel is removed, the display board and "M" multiplier can be removed for repair or replacement.

7.2.4 ANALOG BOARD REMOVAL, REF. FIGURES 7.1, 7.2, and 4.1. Remove the five wire cable assembly to the probe. Remove the bottom cover plate in order to remove the analog board.

Comments:

a. It is recommended that troubleshooting be limited to power supply repair and replacement of defective circuit assemblies.

b. Printed circuit board cleanliness is extremely important when handling high impedance circuits.

c. The analog board has been coated with a protective sealer to minimize the effects of moisture and contamination, however, when handling use plastic gloves.

d. Should troubleshooting down to the component level become necessary, Veeco manufactures a complete set of extender boards and cables for this purpose.

7.3 PROBE HEAD REMOVAL, REF. FIGURE 7.4.

a. Remove the two screws which secure the head adaptor, and unplug the adaptor by sliding it forward.

b. Remove the probe head from the adaptor by removing the head mounting hardware.

c. Unsolder the four head wires, from the connector

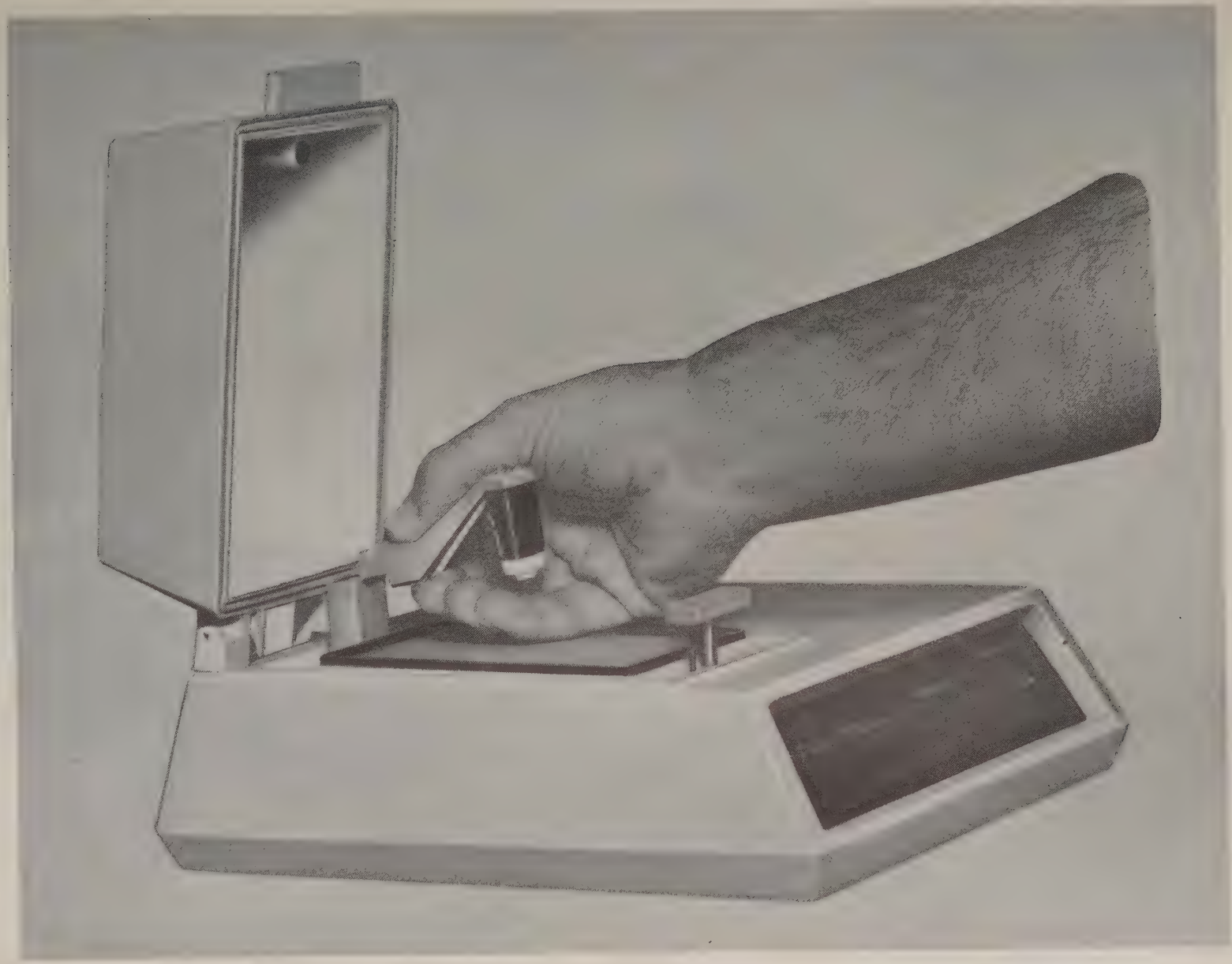


FIGURE 7.4 PROBE HEAD REMOVAL

7.3.1 PROBE HEAD INSTALLATION.

a. Proper orientation is important when soldering probe pins to adaptor connector. Use an ohm-meter to insure proper orientation between probe pins and adapter connector, Ref., Figure 7.5.

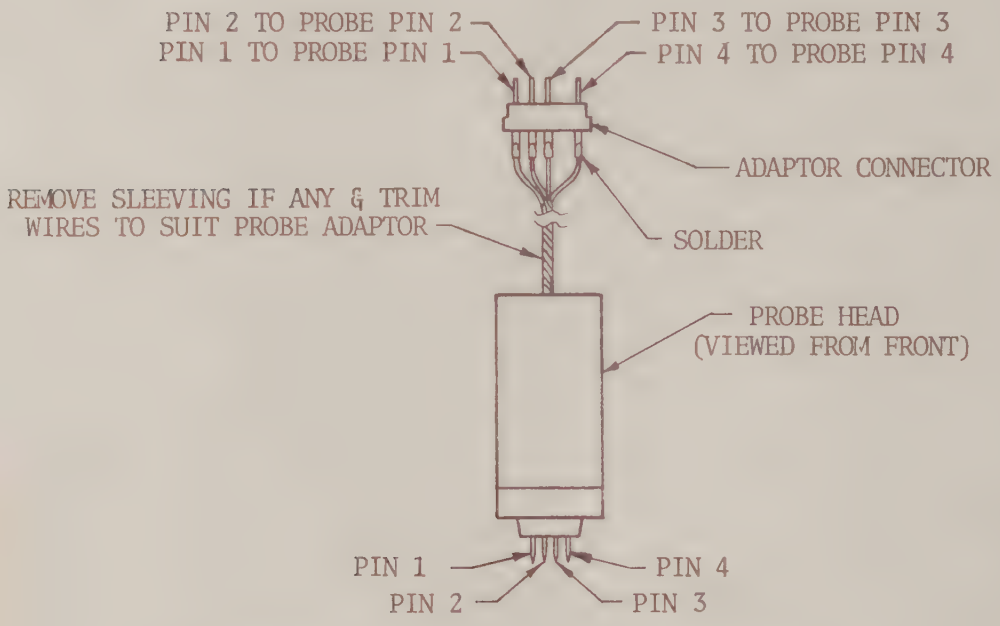

PIN 2 TO PROBE PIN 2
PIN 1 TO PROBE PIN 1
PIN 3 TO PROBE PIN 3
PIN 4 TO PROBE PIN 4
ADAPTOR CONNECTOR
REMOVE SLEEVING IF ANY & TRIM WIRES TO SUIT PROBE ADAPTOR
SOLDER
PROBE HEAD (VIEWED FROM FRONT)
PIN 1
PIN 2
PIN 4
PIN 3

FIGURE 7.5 PROBE HEAD CONNECTOR INSTALLATION.

b. Install new head and connector assembly to the adaptor with mounting hardware.

c. Install head and adaptor assembly to the probe housing using mounting hardware.

7.4 CALIBRATION. Complete information for performing a calibration of the FPP-100 is contained in this section of the manual. Paragraph 7.4.3 describes a calibration check. Paragraph 7.4.4 is the calibration procedure that is used if the calibration check in paragraph 7.4.3 does not give satisfactory results.

7.4.1 EQUIPMENT REQUIRED. The following equipment is required to calibrate the FPP-100:

a. A high input impedance multirange digital voltmeter of 0.1% accuracy or better, with 1 mil volt resolution.

b. Standard resistors: 0.1Ω, 1.0Ω, 10.0Ω, 100.0Ω, 1K, and 10K with value known to within .05%.

c. An insulated blade - type calibration tool.

7.4.2 PREPARATION, REF. FIGURE 7.4.

a. Remove the 2 screws which secure the Probe Adaptor to the probe assembly. Remove the probe adaptor assembly by sliding it forward thus disconnecting the probe connection to the FPP-100 housing.

b. Remove calibration cover. Unsnap the probe simulation cable from its holders, Ref. Figures 3.3, 3.4 and connect it to the probe mating connector.

c. Allow the FPP-100 at least 20 minutes to stabilize at room environment prior to calibration. The unit should not be calibrated if the relative humidity is greater than 50%.

7.4.3 CALIBRATED CHECK.

a. Connect a 1Ω ±.05% standard to the binding posts on the rear panel of the FPP-100 as indicated by Figure 3.5.

b. Select V/I.

c. Press the actuator bar down and hold it down.

d. The display should read between the following limits: 995Ωm to 1.005Ω.

e. With the 1Ω resistor installed, perform the tests as indicated below.

MODE	THICKNESS/RESISTIVITY SETTING	READING FROM	TO	MULTIPLIER
Sheet	Any	4.51	4.55	Ω/sq.
Slice	9.99 x 1 MIL	114.4	115.6	mΩ-cm
Slice	9.99 x 10μ	45.1	45.5	mΩ-cm
Slice	9.99 x 100μ	451	455	mΩ-cm
Thk	9.99 x 1μΩ-cm	219	222	KÅ flash
Thk	9.99 x 100μΩ-cm	21.9	22.2	KÅ
Thk	7.77 x 100μΩ-cm	16.90	17.30	KÅ

f. Connect the .1Ω standard, as in step (a). Select V/I. Measure the resistor by pressing the actuator bar down. The displayed value should be within .5% of the actual resistor value.

g. Repeat the above step (f) using the 10Ω, 100Ω, 1KΩ and 10K resistors. In all cases, the displayed value should be within .5% of the actual resistor value. If the unit fails to pass the preceeding tests, the unit should be calibrated.

7.4.4 CALIBRATION ADJUSTMENT. This calibration procedure should be performed only if the FPP-100 fails to pass the calibration check procedure in Section 7.4.3. The calibration steps in this procedure rely on the preceding steps, therefor care must be taken to make each adjustment in the order that it appears in this procedure. Care must be taken when probing the test points. Probe tips should be insulated so

there is no chance of shorting test point signals to the chassis.

7.4.4.1 ZERO ADJUSTMENT.

a. Place the FPP-100 on its side so the unit is balancing on its cover. Remove the bottom cover, Ref. Figure 4.1.

b. Using a small screwdriver change the position of the "CAL" switch to "CAL MODE" as indicated on the bottom cover.

c. With power on, depress the actuator bar. The display will go blank and the unit will be in the zero state. Perform the following adjustment in the order indicated.

d. Connect the low side of the differential digital voltmeter to "SIG GND", TP16.

e. Monitor TP2. Adjust the input amp pot (V_{xa} course zero) R9 until TP3 is 0 ± 200mV.

f. Monitor TP3. Adjust V_{xa} fine zero pot R21 until TP2 is 0 ± 100μV.

g. Monitor TP10. Adjust V_{sa} zero pot R72 until TP10 is 0 ± 100μV.

h. Monitor TP8. Adjust integrator zero pot R75 until TP8 is 0 ± 100μV.

i. Switch the "CAL" switch from "CAL" to normal. The display will appear.

7.4.4.2 CURRENT SHUNT ADJUSTMENT. To calibrate the FPP-100 current shunt, put the unit into the V/I mode and step through the following procedure to adjust the scale factor for each of the current shunt ranges.

a. Connect the standard 0.1Ω resistor to the binding posts. Press the actuator bar down, and hold it down. Press the retest button down, and adjust the current shunt amp low gain pot R67 until the display reads between the following limits:

99.8 mΩ to 100.2 mΩ

b. Connect the standard 1.00Ω resistor to the binding posts. Adjust the current shunt high gain pot (R70), using the same procedure as above, until the display reads between the following limits:

998. mΩ to 1.002Ω

c. Connect the standard 10.0Ω resistor to the binding posts. Adjust current shunt pot R59 using the same procedure as above, until the display reads between the following limits:

9.98Ω to 10.02Ω

d. Connect the standard 100.0Ω resistor to the binding posts. Varify the display is between the following limits:

99.5Ω to 100.5Ω

If not recheck zero adjustments and do steps A-C again.

e. Connect the standard 1.00KΩ resistor to the binding posts. Adjust current shunt pot R62, using same procedure as before, until the display reads between the following limits:

998Ω to 1002Ω

f. Connect the standard 10.0KΩ resistor to the binding posts. Verify that the display reads between the

following limits:

9.80KΩ to 10.20KΩ

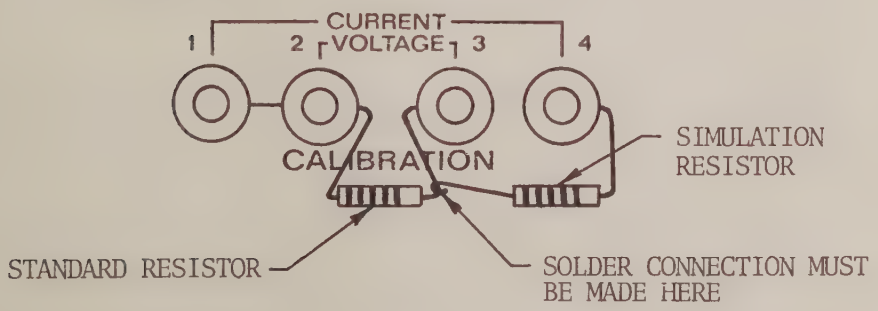
If not recheck zeros and repeat steps A-D.

g. If the unit passes all the preceeding calibration checks, proceed to 7.4.5.

7.4.5 COMMON MODE REJECTION CHECK. The common mode rejection check requires the resistance standards used in 7.4.3 along with the following contact resistance simulation resistors.

1. 100Ω, 1/4w, 5%.
2. 1KΩ, 1/4w 5%.
3. 10KΩ, 1/4w 5%.
4. 100KΩ, 1/4w 5%.
5. 1MΩ, 1/4w 5%.
6. 10MΩ, 1/4w 5%.

a. Connect the .1Ω standard along with the 100Ω load resistor as indicated below. Select V/I.



Push the actuator bar down. The display should read between the following limits.

.0950 mΩ to .1005 mΩ

b. Configure the binding posts as in step (a) using the values below. In all cases the display should read within the accuracy percentage of the standard resistor value as listed below.

STANDARD RESISTOR	SIMULATION RESISTOR	ACCURACY	DISPLAY
1.0	1K 1/4 w 5%.	±0.5%.	.995 -1.005
10.0	10K 1/4 w 5%.	±0.5%.	9.95 -10.05
100.0	100K 1/4 w 5%.	±0.5%.	99.5 -100.5
1.0K	100K 1/4 w 5%.	±0.5%.	995 - 1.005K
1.0K	1Meg 1/4 w 5%.	±3.5%.	965 -1.053K
10.0K	100K 1/4 w 5%.	±2%.	9.80K 10.20K
10.0K	1Meg 1/4 w 5%.	±5%.	9.50K -10.50K

If the unit does not pass the common mode rejection test, the analog board is defective and should be returned to the factory for repair.

7.4.6 TYPE CIRCUIT CHECK. Reinstall the probe head to the FPP-100. Using known P and N type samples. Verify that the unit displays the proper P or N type for both Single and Auto type modes.

7.5 PROBE PRESSURE ZERO ADJUST PROCEDURE, REF. FIGURES 7.6, 7.7.

a. The adaptor and head to be used must be installed. The zero pressure adjustment will vary with the type of probe head being used because of head weights. If a fell type head is installed or any head over 100 grams in weight it will be necessary to remove the chassis from the case, Ref. Paragraph 7.2.1 and reposition the probe counter balance spring, Ref. Figure 7.7.

b. To set zero probe pressure, turn adjustment knob counter clockwise until head will not come down with probe actuator bar depressed.

c. With actuator bar depressed fully, turn zero adjustment knob clockwise until probe tips just clear (by .005 in. or less) substrate holder, release actuator bar.

d. Loosen set screw in zero adjustment knob and while holding zero adjust nut with a suitable wrench, turn knob clockwise or counterclockwise as required so that face of knob is flush or nearly flush with first mark on adjustment rod and zero mark is pointing up (as in Figure 7.6). Tighten set screw.

e. Repeat steps "B" and "C" to double check adjustment. Repeat step "D" if required.

f. Zero adjust is complete.

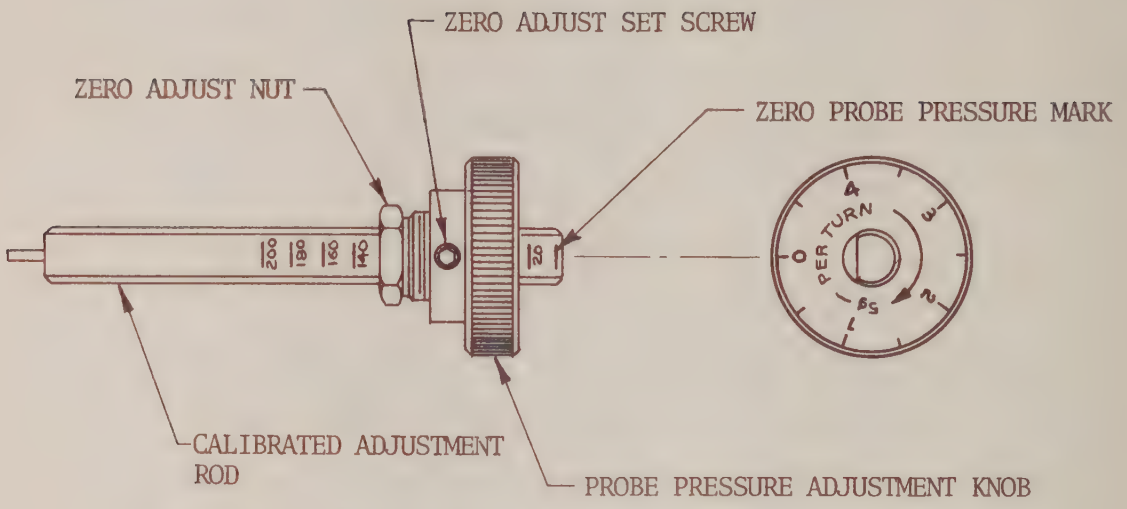


FIGURE 7.6 PROBE PRESSURE ADJUSTMENT KNOB

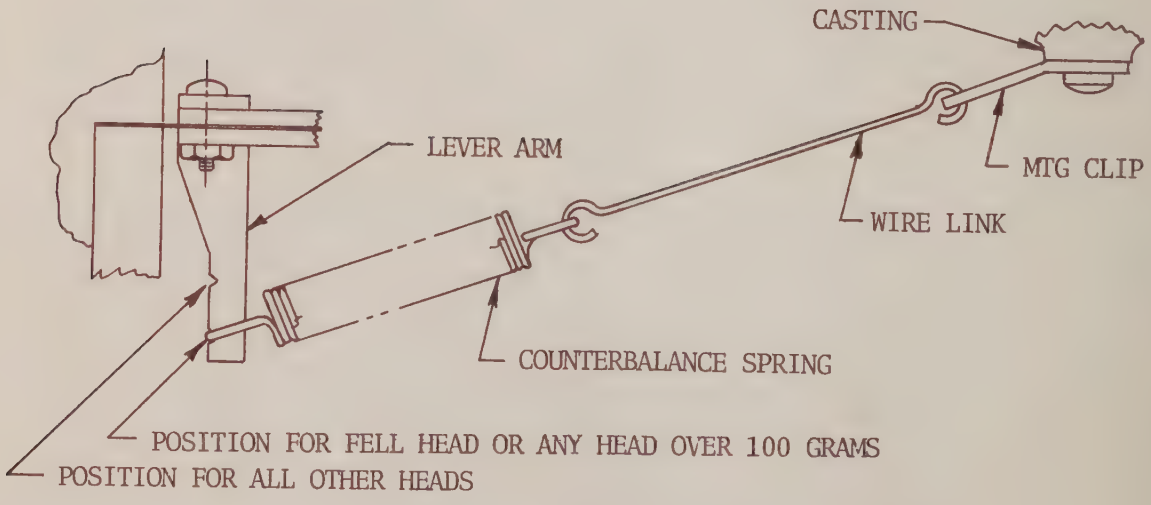


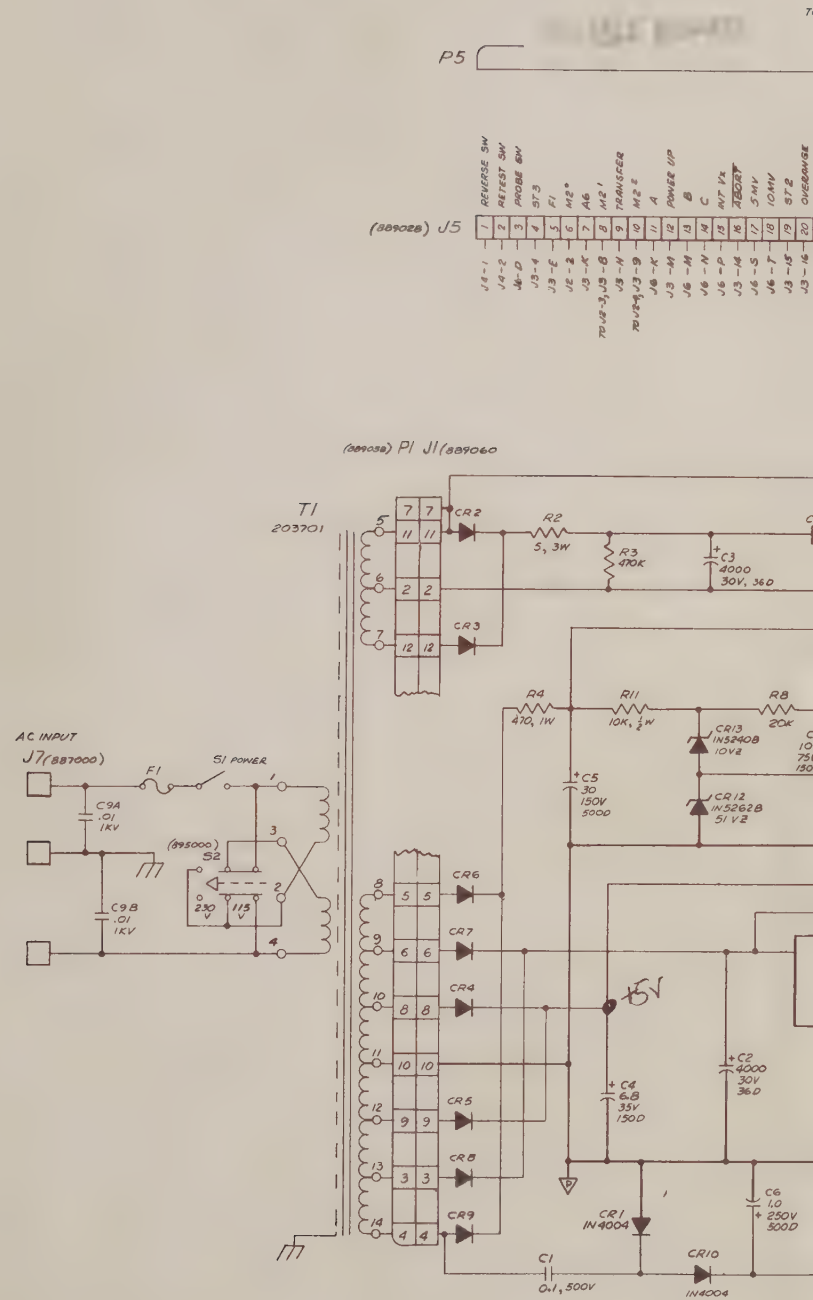
FIGURE 7.7 PROBE HEAD COUNTERBALANCE SPRING

SECTION 8

SCHEMATICS

This section contains a complete set of schematics of all the circuits in the FPP-100. They are arranged in the following order.

Figure 8.1	Power Supply
Figure 8.2	Display Board
Figure 8.3	'M' Multiplier
Figure 8.4	Digital Board I
Figure 8.5	Digital Board II
Figure 8.6	Analog Board


P5
(889028) J5
REVERSE SW
RETEST SW
PROBE 6V
ST3
F1
H12°
A6
H12 1
TRANSFER
H12 2
A
POWER UP
B
C
R/T V2
ABORT
5 MV
10 MV
ST2
OVERRANGE
J4-1
J4-2
J4-D
J3-4
J3-E
J2-2
J3-K
J3-B
J3-N
J3-9
J6-K
J3-M
J6-M
J6-N
J6-P
J3-14
J6-S
J6-T
J3-13
J3-16
(889038) P1 J1(889060
T1
203701
CR2
CR3
R2
5, 3W
R3
470K
C3
4000
30V, 36D
R4
470, 1W
R11
10K, ½W
R8
20K
CR13
IN5240B
10V2
CR12
IN5262B
51 V2
C5
30
150V
500D
AC INPUT
J7(887000)
F1
S1 POWER
C9A
.01
1KV
C9B
.01
1KV
(895000)
S2
230 V
115 V
CR6
CR7
CR4
CR5
CR8
CR9
+5V
C4
6.8
35V
150D
C2
4000
30V
36D
C6
1.0
250V
500D
CR1
IN4004
CR10
IN4004
C1
0.1, 500V

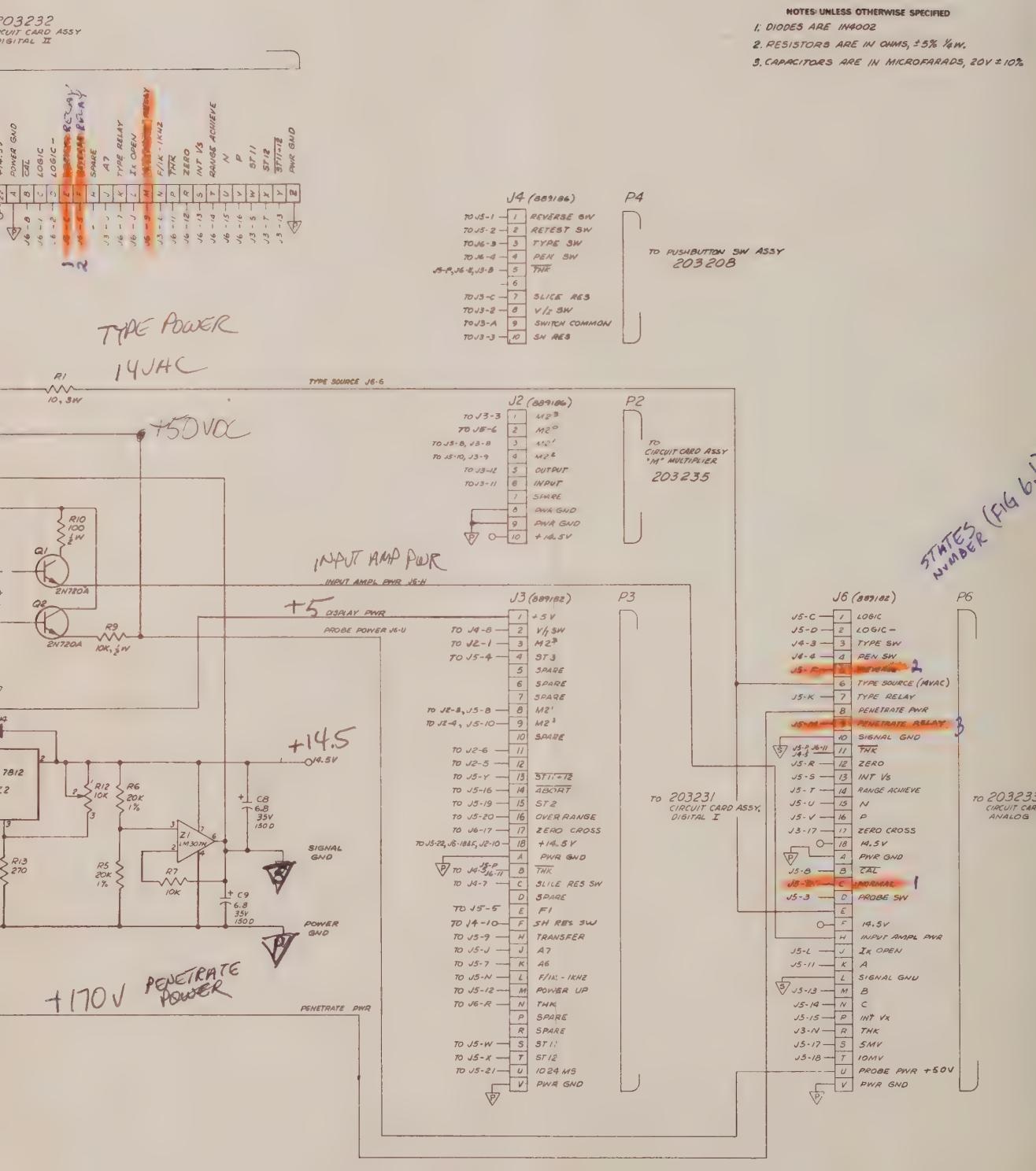


FIGURE 8.1 POWER SUPPLY SCHEMATIC

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE COMPOSITION, $\frac{1}{2}$W ±5%, 200Ω.
2. DASH LINE REPRESENTS WIRING SEE DWG NO. 203202.

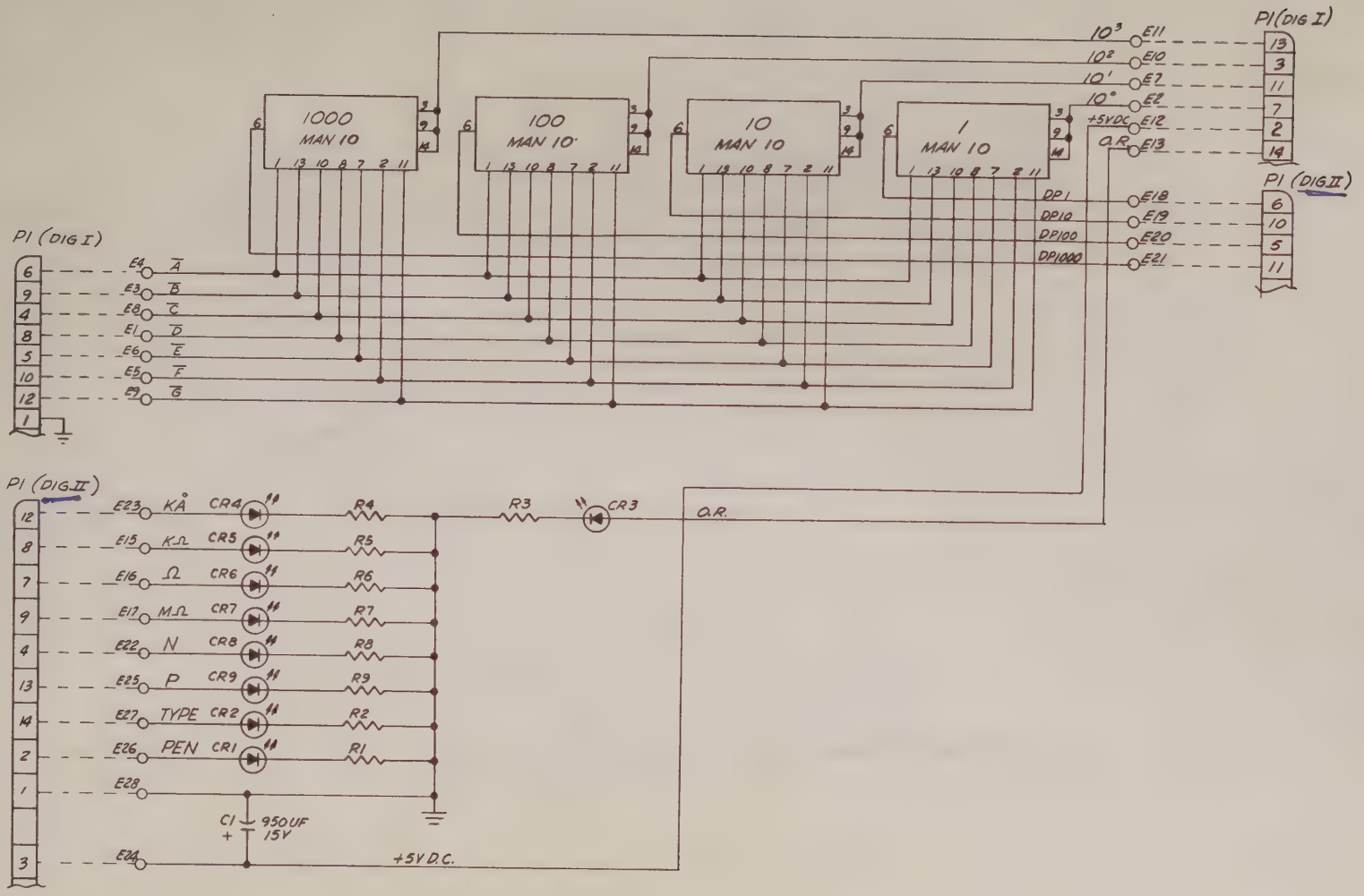


FIGURE 8.2 DISPLAY BOARD SCHEMATIC

NOTES: UNLESS OTHERWISE SPECIFIED

1. DOTTED LINES REPRESENTS WIRE HARNESS SEE DWG 203210.
2. RESISTORS ARE COMPOSITION 560K OHMS ¼W ±5%

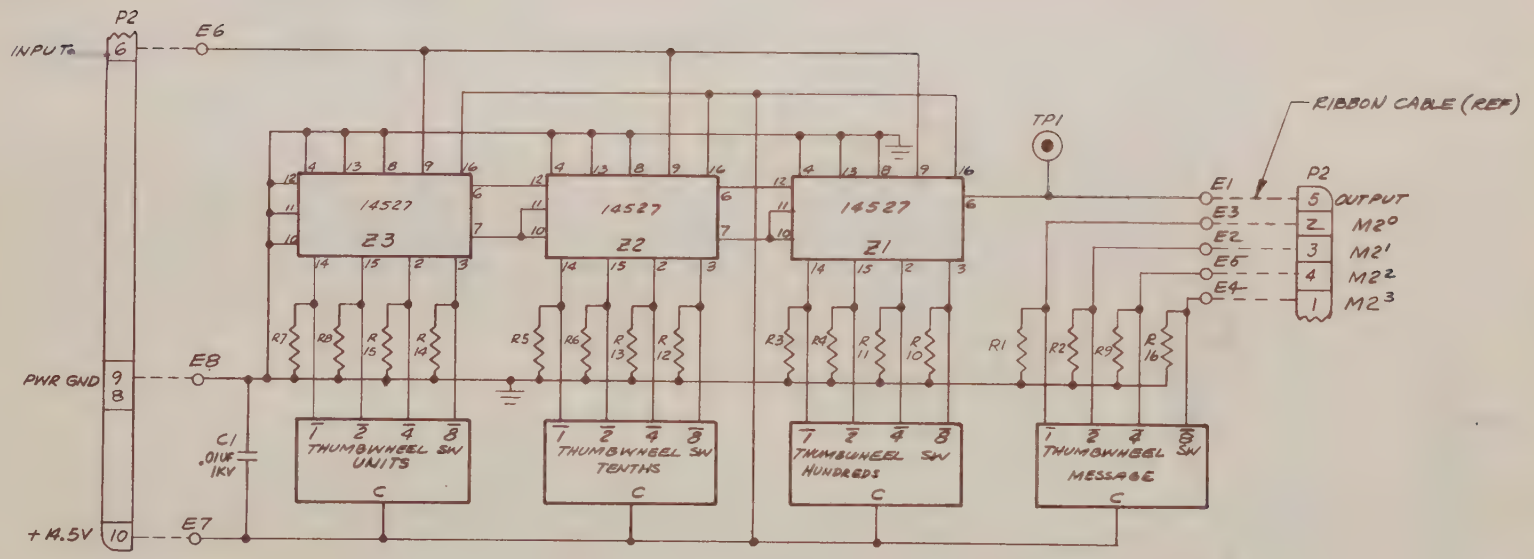
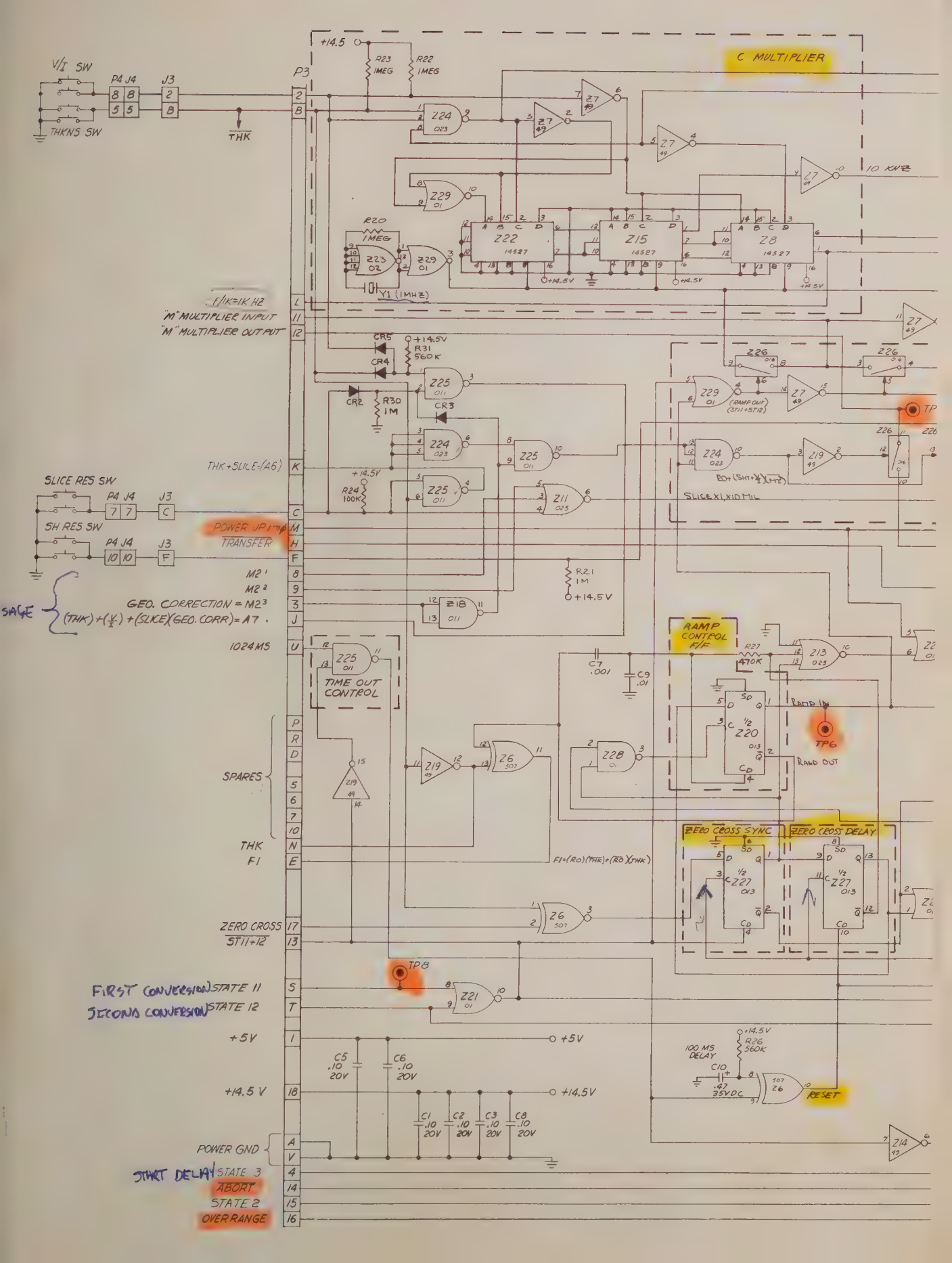
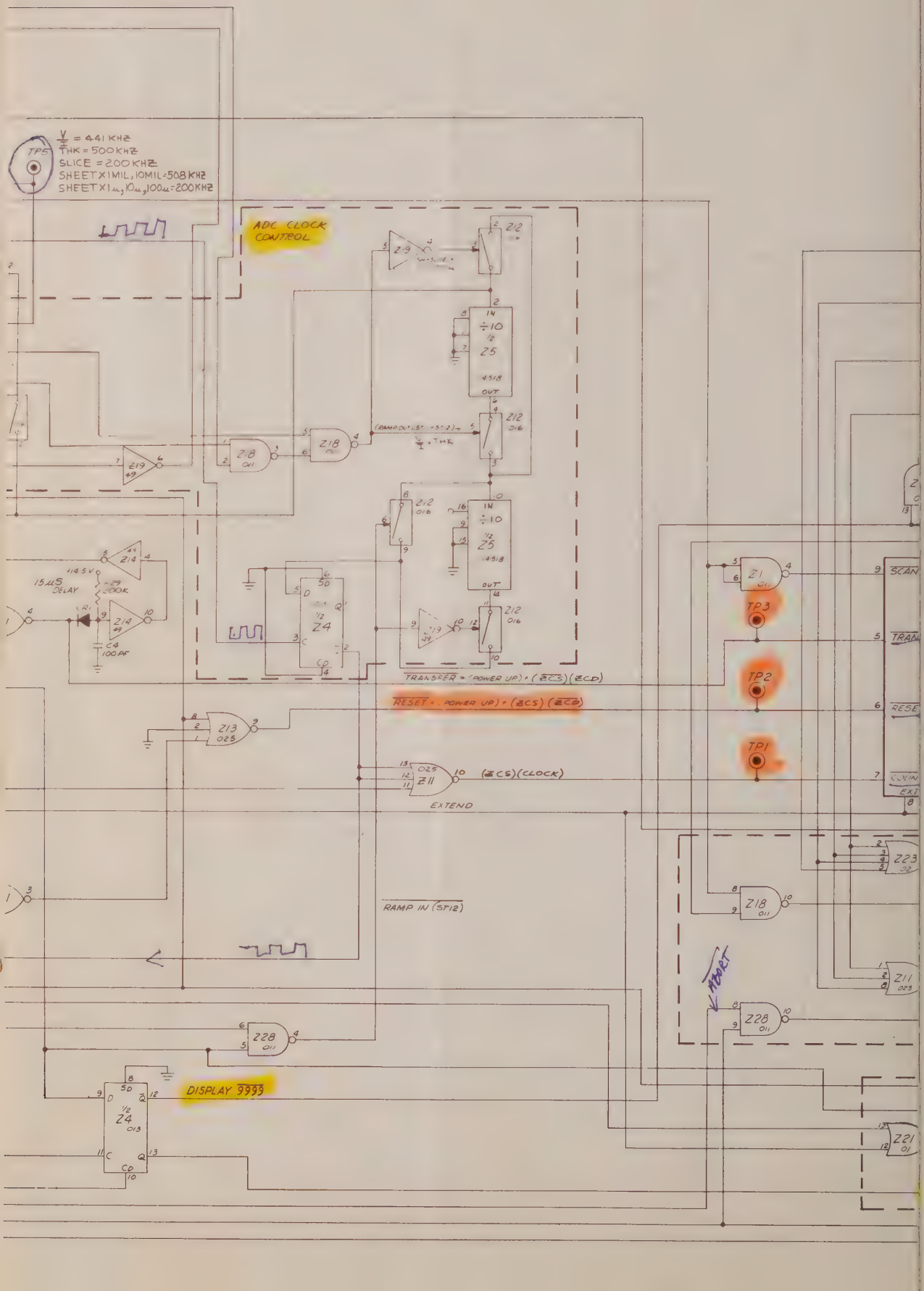
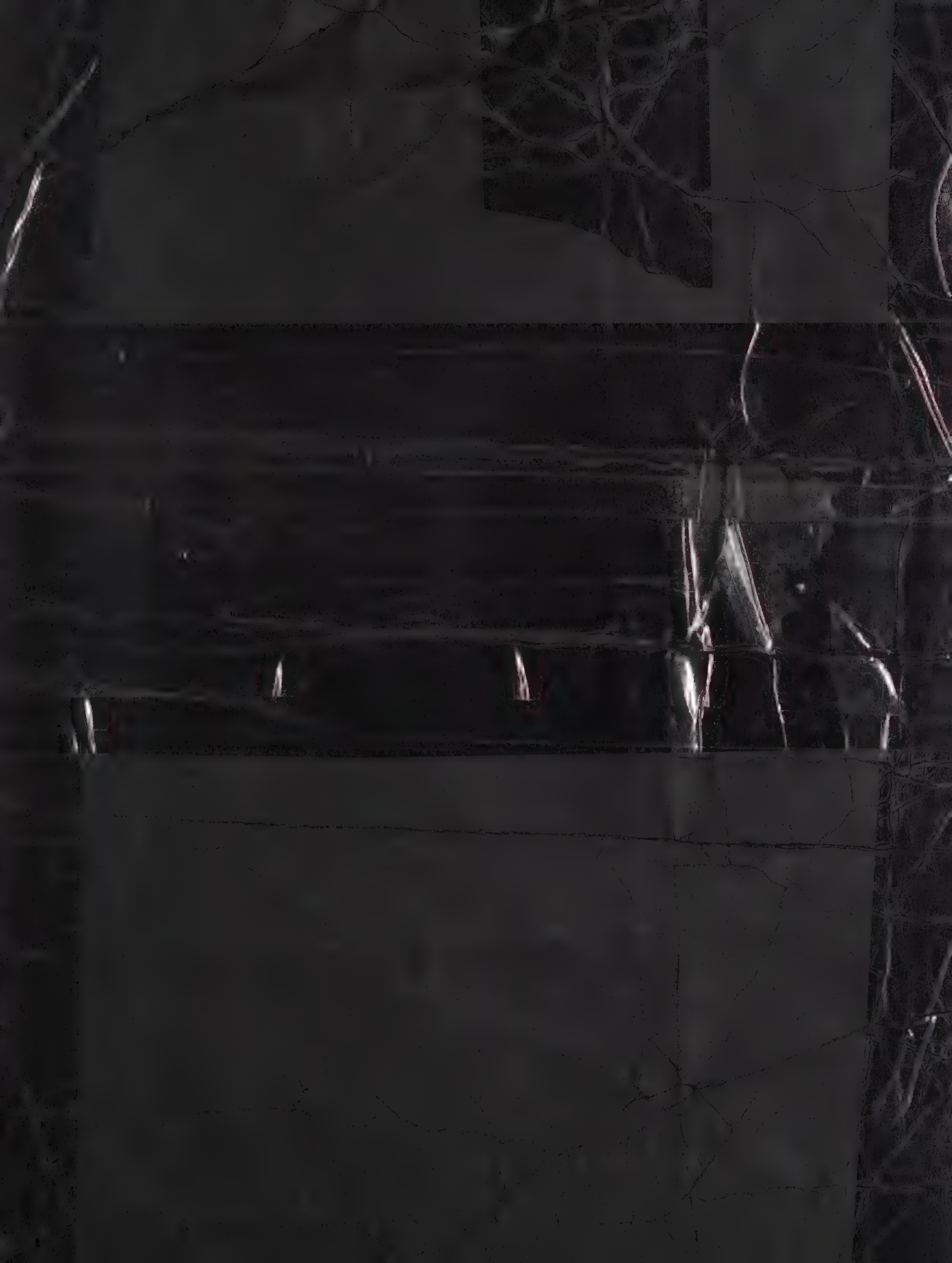
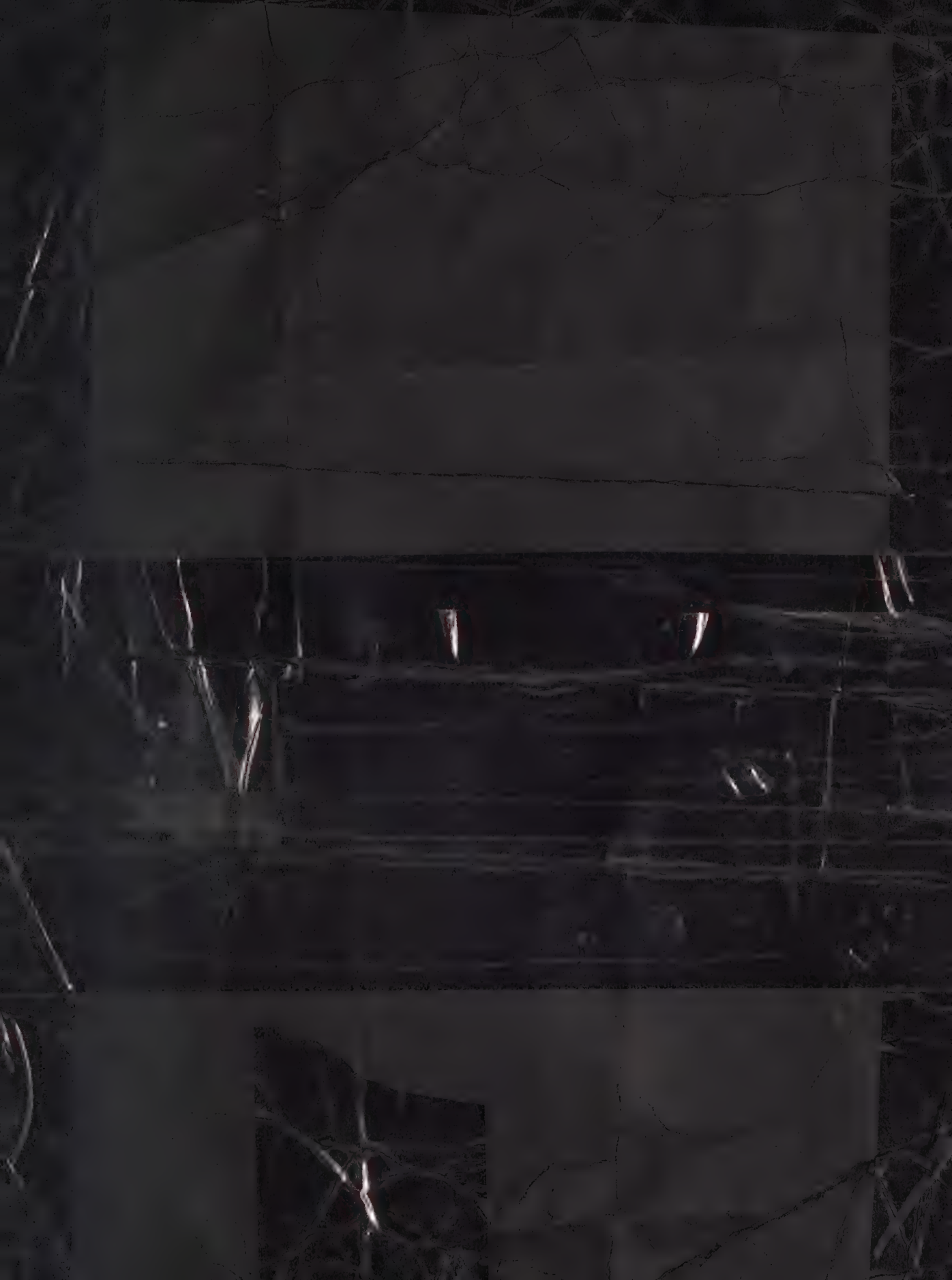


FIGURE 8.3 'M' MULTIPLIER SCHEMATIC


C MULTIPLIER
V/I SW
THKNS SW
THK
P3
+14.5
R23 1MEG
R22 1MEG
10 KHZ
R20 1MEG
Y1 (1MHZ)
F/IK=1K HZ
"M" MULTIPLIER INPUT
"M" MULTIPLIER OUTPUT
CR5
CR4
CR2
CR3
R31 560K
R30 1M
R24 100K
R21 1M
THK + SLICE = (A6)
SLICE RES SW
SH RES SW
POWER UP RESET
TRANSFER
M2'
M2²
GEO. CORRECTION = M2³
(THK) + (½) + (SLICE)(GEO. CORR) = A7
1024 MS
TIME OUT CONTROL
RAMP CONTROL F/F
R27 470K
C7 .001
C9 .01
RAMP IN
RAMP OUT
TP6
TP8
SPARES
THK
F1
F1=(R0)(THR)+(R0)(THK)
ZERO CROSS
ST11+12
ZERO CROSS SYNC
ZERO CROSS DELAY
FIRST CONVERSION STATE 11
SECOND CONVERSION STATE 12
+5V
+14.5 V
C5 .10 20V
C6 .10 20V
C1 .10 20V
C2 .10 20V
C3 .10 20V
C8 .10 20V
100 MS DELAY
R26 560K
C10 .47 35VDC
RESET
POWER GND
START DELAY STATE 3
ABORT
STATE 2
OVER RANGE


TP5
V/THK = 4.41 KHZ
THK = 500 KHZ
SLICE = 200 KHZ
SHEET X1 MIL, 10 MIL = 508 KHZ
SHEET X1 μ, 10 μ, 100 μ = 200 KHZ
ADC CLOCK CONTROL
Z19
Z12
Z5
÷10
Z18
Z8
Z14
1.4 SV
15 μS DELAY
R1
C4 100 PF
Z4
Z13
Z11
EXTEND
(ECS)(CLOCK)
TRANSFER = (POWER UP) + (ECS)(ECD)
RESET = (POWER UP) + (ECS)(ECD)
RAMP IN (ST12)
DISPLAY 9999
Z28
Z1
TP3
TP2
TP1
SCAN
RESET
Z23
Z18
Z11
Z21
RESET





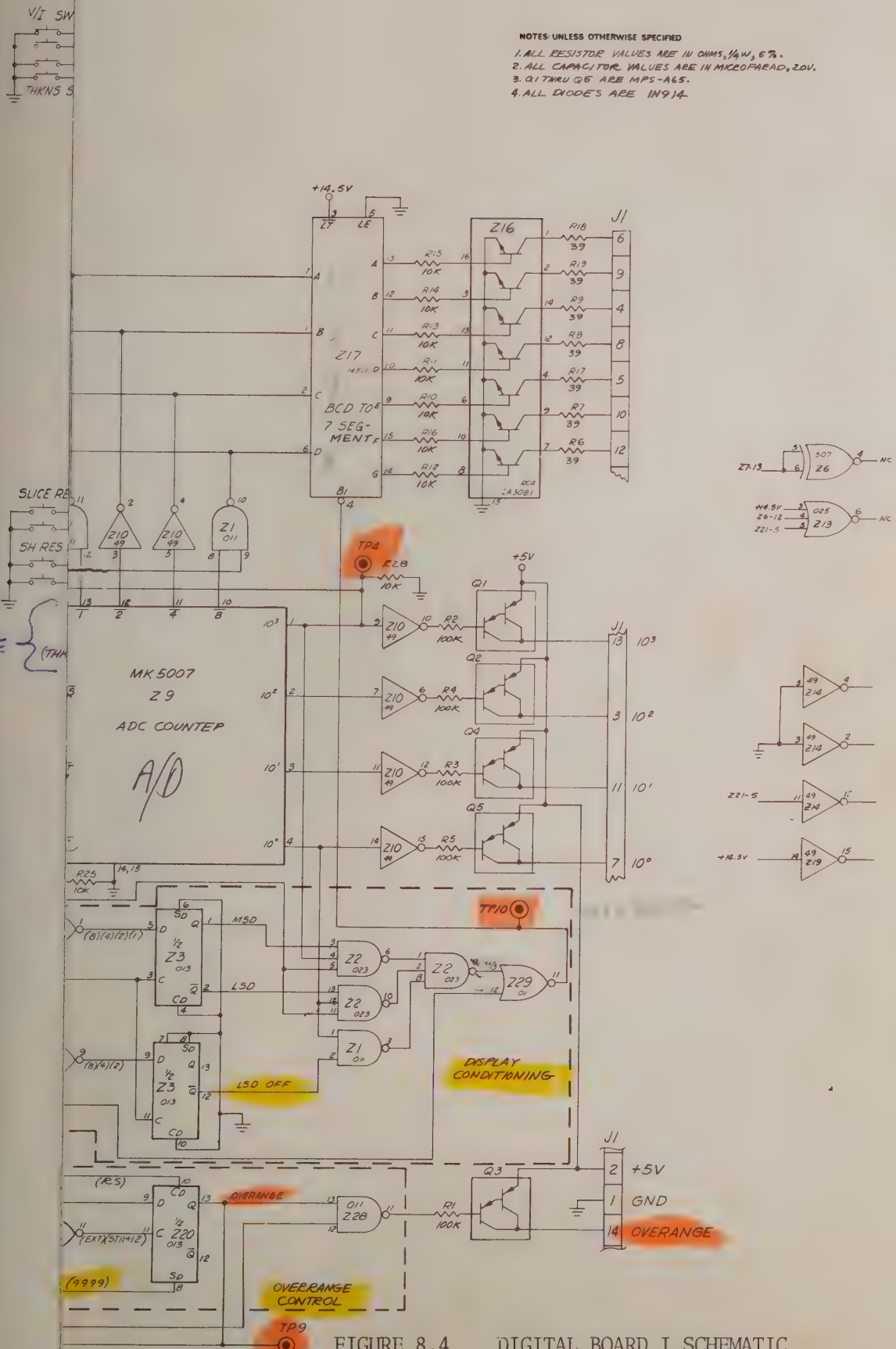
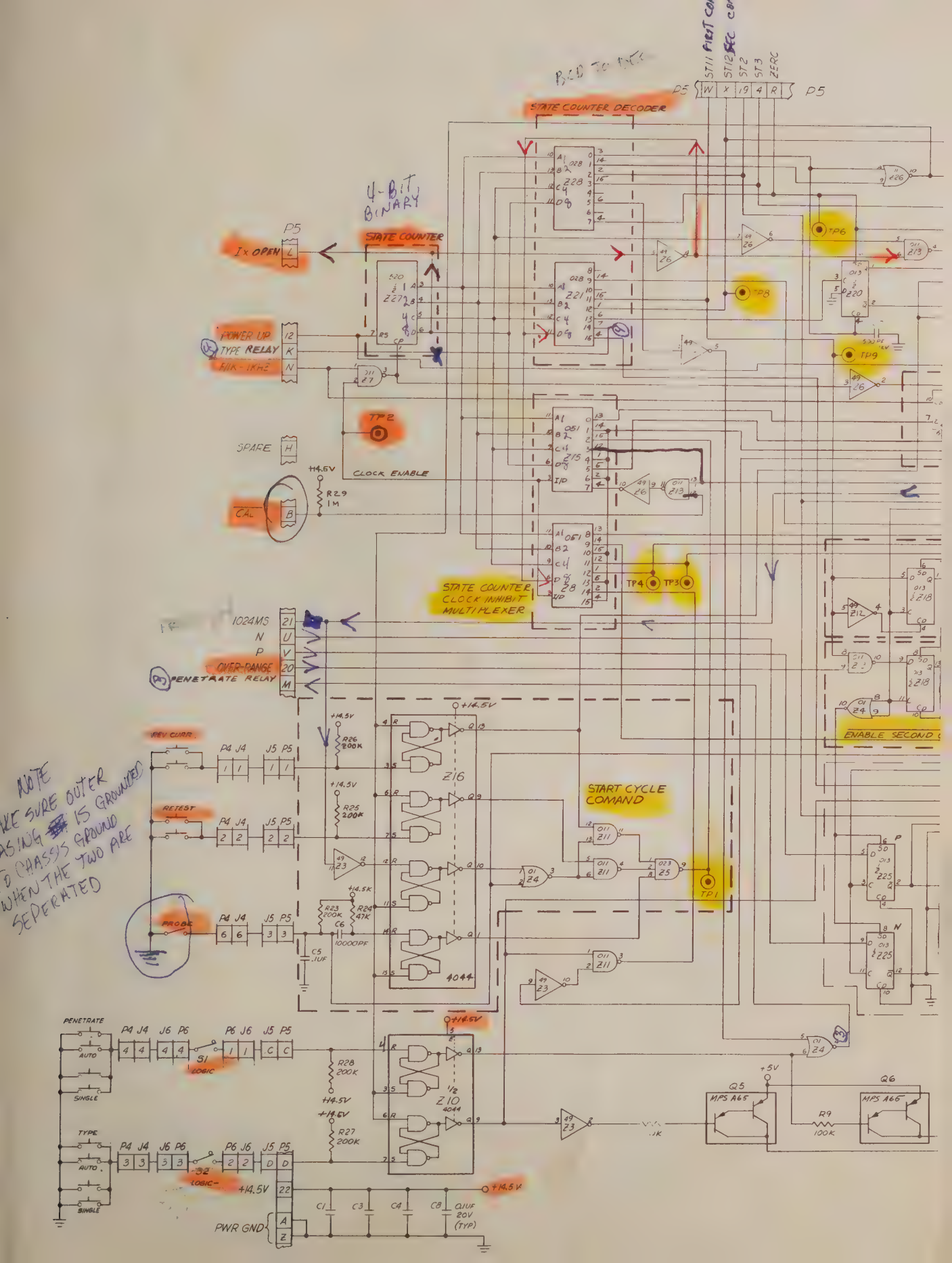
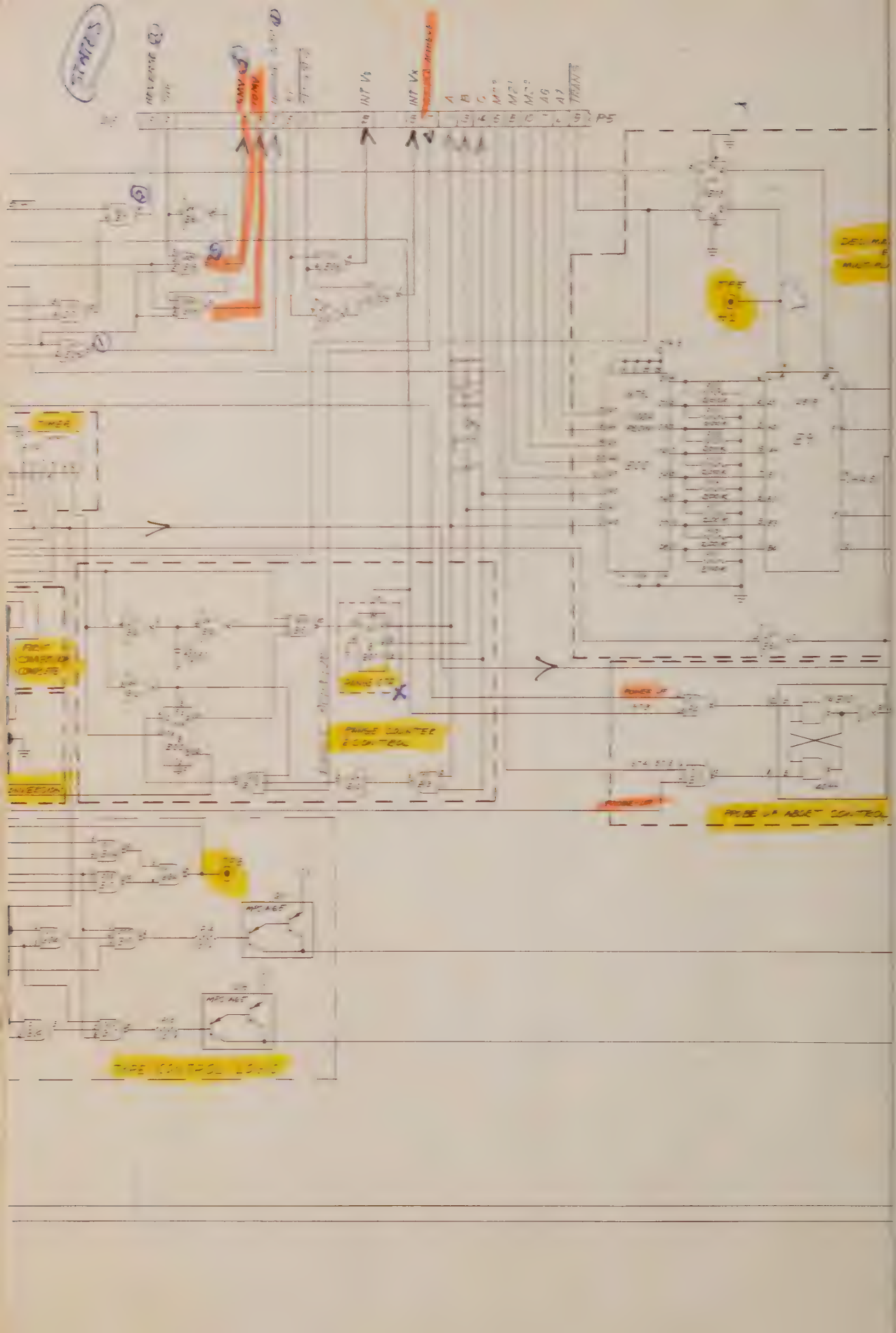
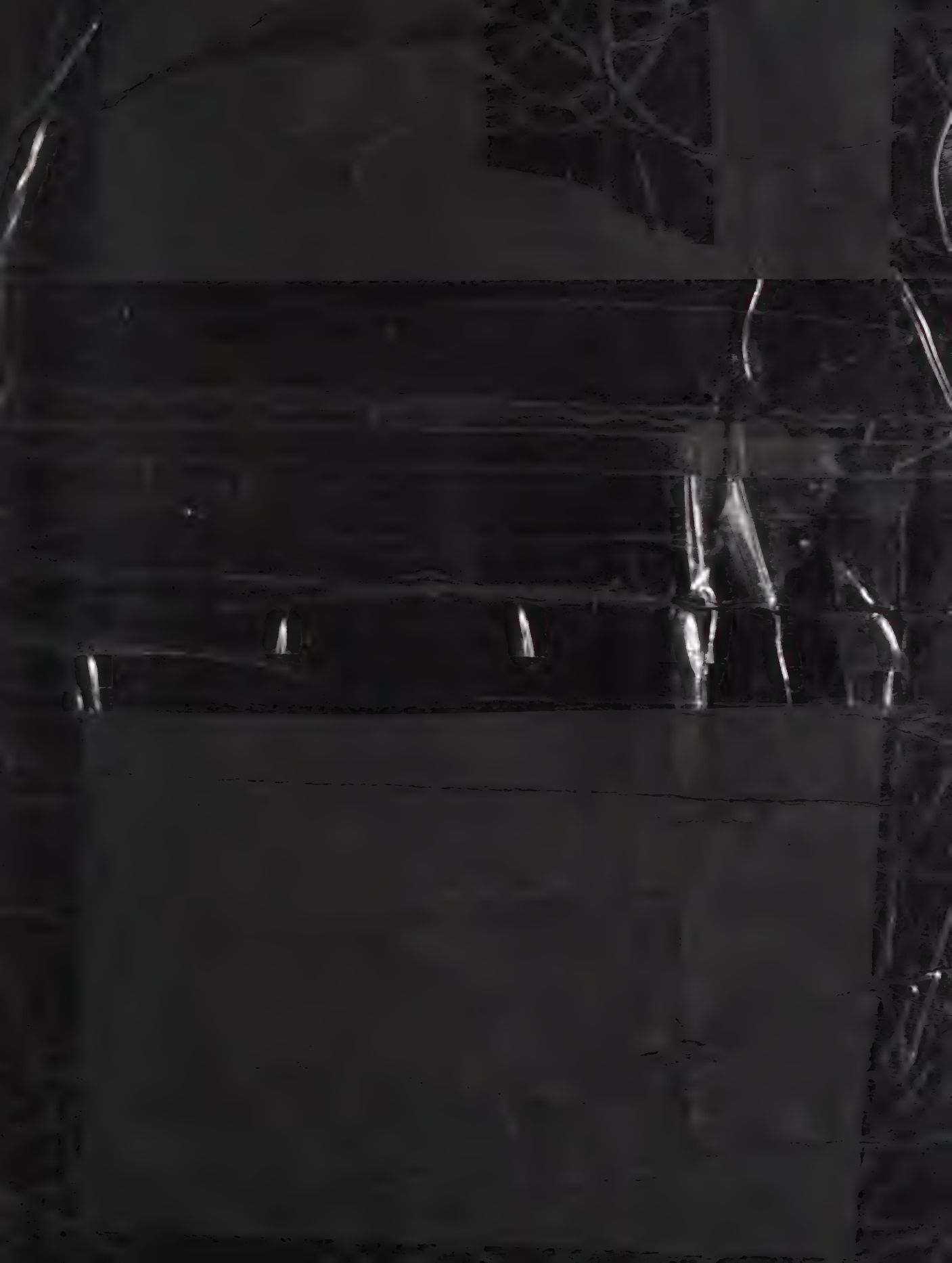


FIGURE 8.4 DIGITAL BOARD I SCHEMATIC


STATE COUNTER DECODER
4-BIT BINARY
STATE COUNTER
P5
I x OPEN
POWER UP
TYPE RELAY
5/1K - 1KHz
SPARE
CAL
+14.5V
R29 1M
TP2
CLOCK ENABLE
STATE COUNTER CLOCK INHIBIT MULTIPLEXER
TP4
TP3
1024MS
OVER-RANGE
PENETRATE RELAY
REV CURR
RETEST
PROBE
R26 200K
R25 200K
R23 200K
R24 47K
C6 10000PF
C5 .1UF
Z16
4044
START CYCLE COMAND
TP1
ENABLE SECOND
PENETRATE
AUTO
SINGLE
S1
LOGIC
R28 200K
R27 200K
Z10
TYPE
S2
Q5
MPS A65
Q6
R9 100K
+5V
PWR GND
C1
C3
C4
C8 .01UF 20V (TYP)
NOTE
MAKE SURE OUTER CASING IS GROUNDED TO CHASSIS GROUND WHEN THE TWO ARE SEPERATED


TIMER
PURGE COUNTER & CONTROL
PROBE UP ABORT CONTROL
TUBE CONTROL LOGIC



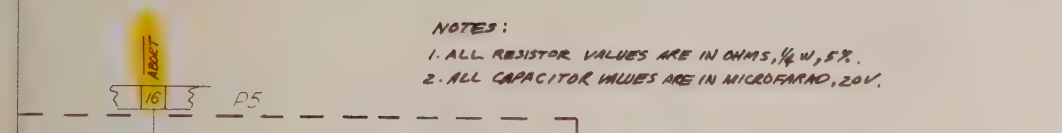
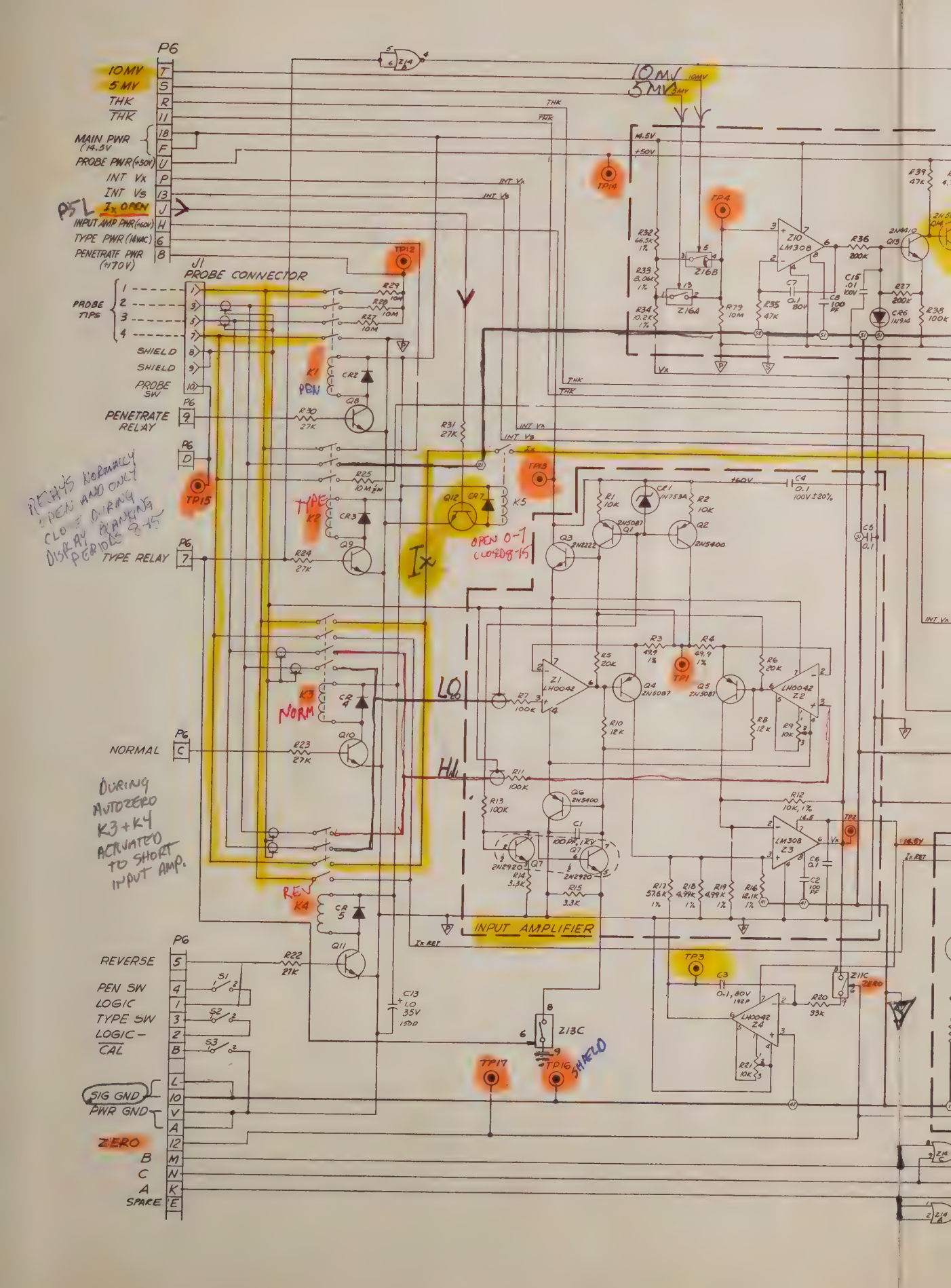
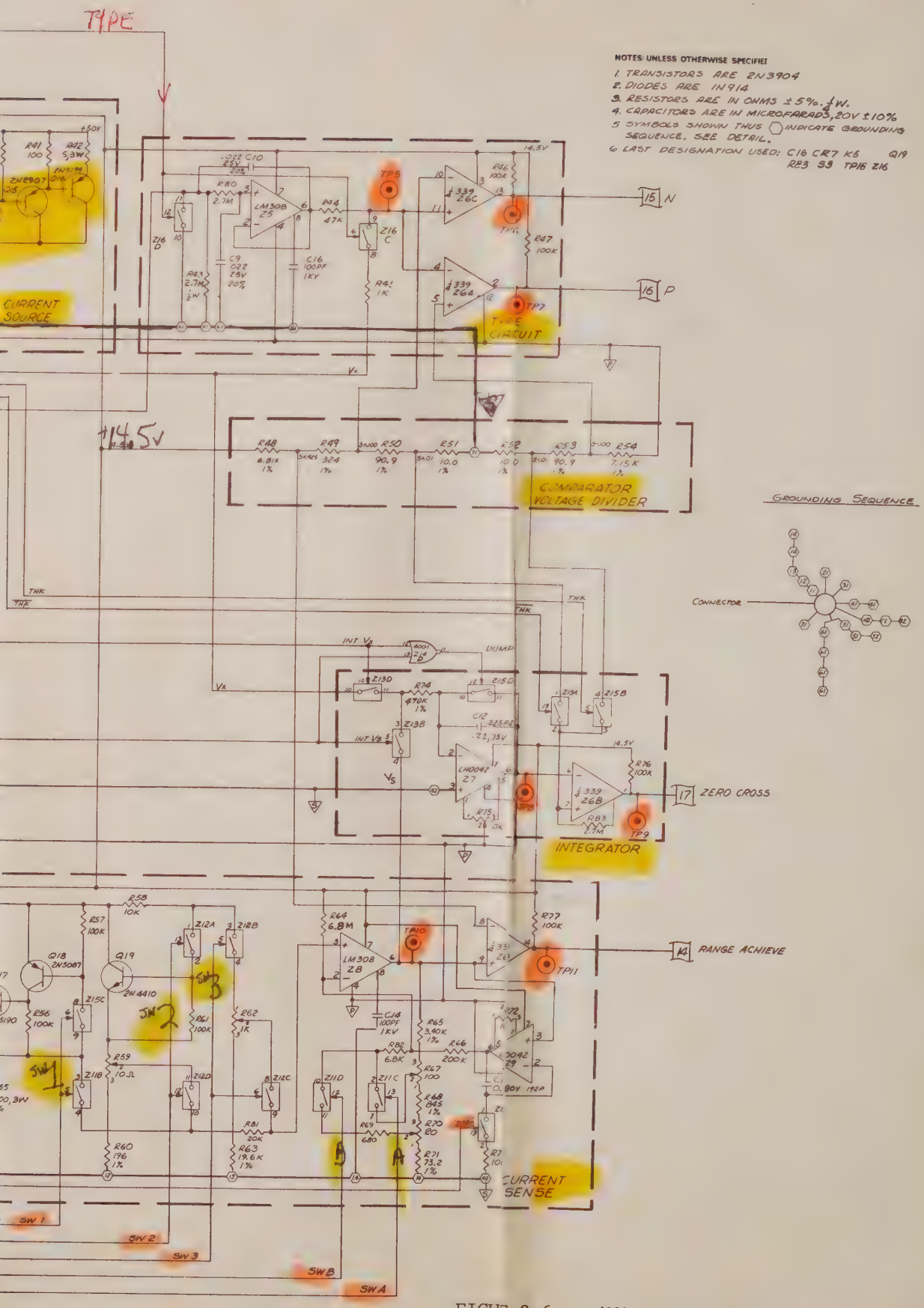


FIGURE 8.5 DIGITAL BOARD II SCHEMATIC


P6
10MV
5MV
THK
THK
MAIN PWR (14.5V)
PROBE PWR (+50V)
INT Vx
INT Vs
Ix OPEN
INPUT AMP PWR (+60V)
TYPE PWR (16VAC)
PENETRATE PWR (+170V)
J1 PROBE CONNECTOR
PROBE TIPS
SHIELD
SHIELD
PROBE SW
PENETRATE RELAY
TYPE RELAY
NORMAL
REVERSE
PEN SW
LOGIC
TYPE SW
LOGIC – CAL
SIG GND
PWR GND
ZERO
B
C
A
SPARE
PENETRATE NORMALLY OPEN AND ONLY CLOSE DURING DISPLAY PERIODS
K1 PEN
K2 TYPE
K3 NORM
K4 REV
K5
Ix
OPEN 0-7 CLOSED 8-15
LO
HI
DURING AUTOZERO K3+K4 ACTIVATED TO SHORT INPUT AMP.
INPUT AMPLIFIER
Ix RET
SHIELD
+50V
+60V
14.5V
INT Vx
INT Vs
THK
10MV
5MV
TP1
TP2
TP3
TP4
TP12
TP13
TP14
TP15
TP16
TP17
Z1 LH0042
Z2 LH0042
Z3 LM308
Z4 LH0042
Z10 LM308
Z16A
Z16B
Z13C
Z11C
Q1 2N5087
Q2 2N5400
Q3 2N2222
Q4 2N5087
Q5 2N5087
Q6 2N5400
Q7 2N2920
Q8
Q9
Q10
Q11
Q12
CR1 IN753A
CR2
CR3
CR4
CR5
CR6 IN914
CR7
S1
S2
S3
C1 100 PF, 1KV
C2 100 PF
C3 0.1, 80V 1%2D
C4 0.1 100V ±20%
C5 0.1
C6 0.1
C7 0.1 80V
C8 100 PF
C13 10 35V 15%D
C15 .01 100V
R1 10K
R2 10K
R3 49.9 1%
R4 49.9 1%
R5 20K
R6 20K
R7 100K
R8 12K
R9 10K
R10 12K
R11 100K
R12 10K, 1%
R13 100K
R14 3.3K
R15 3.3K
R16 12.1K 1%
R17 57.6K 1%
R18 4.99K 1%
R19 4.99K 1%
R20 33K
R21 10K
R22 27K
R23 27K
R24 27K
R25 10M ¼W
R27 10M
R28 10M
R29 10M
R30 27K
R31 27K
R32 66.5K 1%
R33 8.06K 1%
R34 10.2K 1%
R35 47K
R36 200K
R37 200K
R38 100K
R39 47K
R79 10M
Q13 2N4410
CR6 IN914



FIGUE 8.6 ANALOG BOARD SCHEMATIC

SECTION 9

PARTS LIST

This is a list of all electronic parts that are used in the unit. They are listed according to the boards on which they are used.

9.1 DISPLAY BOARD ASSEMBLY, 203202.

DESIGNATOR	KRONOS P/N	DESCRIPTION
1	897015	MAN 10A LED
10	897015	MAN 10A LED
100	897015	MAN 10A LED
1000	897015	MAN 10A LED
CR1-9	879018	MV 5023 LED
C1	981795	CAP, 950 µf, 15 VDC
R1-9	999120	RES, 200 Ω, 1/4 w 5%.

9.2 CHASSIS ASSEMBLY, 203209.

T1	203701	Transformer
F1	869005	Fuse 5A, 313, 3AG

9.3 POWER SUPPLY BOARD ASSEMBLY, 203234.

C1	989410-500	Disk 0.1 mf 500V
C2,3	983840-30	Elec 4000 mf 30V
C4	981568-35	Tant 6.8 µf, 35V
C5	981630-150	Elec 30 mf 250V
C6	981510-250	Elec 1 mf 250V
C7	981610-75	Tant 10 mf 75V
C8,9	981568-35	Tant 6.8 µf 35V
CR1	974004	Diode IN4004
CR2-9	974002	Diode IN4002
CR10	974004	Diode IN4004
CR11	974002	Diode IN4002
CR12	975262B	Zener 51VIN5262B

DESIGNATOR	KRONOS P/N	DESCRIPTION
CR13	975240B	Zener 10VIN5240B
CR14	974002	Diode IN4002
R1	995010	10 3 w
R2	995005	5 3 w
R3	999447	470K 1/4 w 5%
R4	997147	470 1 w 5%
R5,6	991320	20K 1/8 w 1%
R7	999310	10K 1/4 w 5%
R8	999320	20K 1/4 w 5%
R9	998310	10K 1/2 w 5%
R10	998110	100 1/2 w 5%
R11	998310	10K 1/2 w 5%
R12	990310	Pot Bourns 10K 3339P
R13	999127	270 1/4 w 5%
Z1	950307N	ICLM307N
Z2	957812	REGNC 7812
Q1,2	960720A	Tran 2N720A
J1	889058	Wafer Conn 12 pin
J2	889183	Wafer Conn 12 pin
J3	889182	Conn 36 pin
J4	889183	Wafer Conn
J5	889028	Conn 44 pin
J6	889182	Conn 36 pin

9.4 M MULTIPLIER ASSEMBLY, 203235.

R1-16	999456	Resistor 560K 1/4 w 5%
Z1,2,3	921452.7	IC 14527
S1	203700	Thumbwheel switch assy

9.5 DIGITAL BOARD I ASSEMBLY, 203231.

Z1	924011	IC CD 4011
Z2	924023	IC CD 4023
Z3,4	924013	IC CD 4013
Z5	921451-8	IC MC 14518
Z6	921450-7	IC MC 14507
Z7	924049	IC CS 4049
Z8	921452-7	IC MC 14527
Z9	889026	Socket 16 pin
Z9 socket	935007	Mostek IC 5007
Z10	924049	IC CD 4049
Z11	924025	IC CD 4025
Z12	921401-6	IC MC 14016

DESIGNATOR	KRONOS P/N	DESCRIPTION
Z13	924025	IC CD 4025
Z14	924049	IC CD 4049
Z15	921452-7	IC MC 14527
Z16	913081	IC CA 3081
Z17	921451-1	IC MC 14511
Z18	924011	IC CS 4011
Z19	924049	IC CD 4049
Z20	924013	IC CD 4013
Z21	924001	IC CS 4001
Z22	921452-7	IC MC 14527
Z23	924023	IC CD 4023
Z24	924023	IC CD 4023
Z25	924011	IC CD 4011
Z26	921401-6	IC MC 14016
Z27	924013	IC CD 4013
Z28	924011	IC CD 4011
Z29	924001	IC CD 4001
R1-5	999410	Res 100K 1/4 w 5%
R6-9	999039	Res 39 Ω 1/4 w 5%
R10-16	999310	Res 10K 1/4 w 5%
R17-19	999039	Res 39 Ω 1/4 w 5%
R20-23	999510	Res 1 Meg 1/4 w 5%
R24	999410	Res 100K 1/4 w 5%
R25	999310	Res 10K 1/4 w 5%
R26, 31	999456	Res 560K 1/4 w 5%
R27	999427	Res 470K 1/4 w 5%
R28	999310	Res 10K 1/4 w 5%
R29	999420	Res 200K 1/4 w 5%
R30	999501	Res 1 Meg 1/4 w 5%
C1-3	988410-20	Disc 0.1 mf 20V
C4	988110-1K	Disc 100 pf 1KV
C5,6	988410-20	Disc 0.1 mf 20V
C7	988210-1K	Disc .001 mf 1KV
C8	988410-20	Disc 0.1 mf 20V
C9	988310-100	Disc .01 mf
C10	981447-35	Tant 0.47 mf 35V
Q1-5	960065	Tran MSPA 65
CR1-5	970914	Diode IN 914
J1	889027	Socket 14 pin
Y1	858100	Crystal 1.000 mHz

9.6 DIGITAL BOARD II ASSEMBLY, 203232.

Z1	921455-5	IC MC 14555

DESIGNATOR	KRONOS P/N	DESCRIPTION
Z2	924011	IC CD 4011
Z3	924049	IC CS 4049
Z4	924001	IC CD 4001
Z5	924023	IC CD 4023
Z6	924049	IC CD 4049
Z7	924011	IC CD 4011
Z8	924051	IC CD 4051
Z9	921451-9	IC MC 14519
Z10	924044	IC CD 4044
Z11	924011	IC CD 4011
Z12	924049	IC CD 4049
Z13	924011	IC CD 4011
Z14	921404-0	IC MC 14040
Z15	924044	IC CD 4051
Z16	924044	IC CD 4044
Z17	924023	IC CD 4023
Z18	924013	IC CD 4013
Z19	924025	IC CD 4025
Z20	924013	IC CD 4013
Z21	921402-8	IC MC 14028
Z22 socket	889208	Socket 24 pin
Z22	931702	IC from 1702
Z23	924013	IC CD 4013
Z24	924011	IC CD 4011
Z25	924013	IC CD 4013
Z26	924001	IC CD 4001
Z27 socket	889026	Socket 16 pin
Z27	921452-0	MC 14520
Z28	921402-8	IC MC 14028
R1	999410	Res 100K 1/4 w 5%
R2	999110	Res 100 Ω 1/4 w 5%
R3,4	999347	Res 47K 1/4 w 5%
R5	999110	Res 100 Ω 1/4 w 5%
R6	999347	Res 47K 1/4 w 5%
R7	999110	Res 100 Ω 1/4 w 5%
R8-14	999410	Res 100K 1/4 w 5%
R15-23 25, 26	999420	Res 200K 1/4 w 5%
R24	999347	Res 100K 1/4 w 5%
R27,28	999420	Res 200K 1/4 w 5%
R29	999510	Res 1 Meg 1/4 w 5%
C1	998410-20	Disc 0.1 mf 20V
C2	989150-1K	Disc 500 pf 1KV
C3-5	988410-20	Disc 0.1 mf 20V
C6	988310-100	Disc .01 mf 100V
C7	989150-1K	Disc 500 pf 1KV
C8	988410-20	Disc 0.1 mf 20V
Q1	960065	Tran MSPA 65
Q2-4	963904	Tran 2N 3904
Q5-11	960065	Tran MSPA65

DESIGNATOR	KRONOS P/N	DESCRIPTION
J1	889027	Socket 14 pin

9.7 ANALOG BOARD ASSEMBLY, ~~203233.~~ 8203-233 - $9.90.00

R1,2	999310	Res 10K 1/4 w 5%
R3,4	991049.9	Res 49.9 1/8 w 1%
R5,6	999320	Res 20K 1/4 w 5%
R7	999410	Res 100K 1/4 w 5%
R8	999312	Res 12K 1/4 w 5%
R9	990310	Pot 10K
R10	999312	Res 12K 1/4 w 5%
R11	999410	Res 100K 1/4 w 5%
R12	991310	Res 10K 1/8 w 1%
R13	999410	Res 100K 1/4 w 5%
R14,15	999233	Res 3.3K 1/4 w 5%
R16	991312.1	Res 12.1K 1/8 w 1%
R17	991357.6	Res 57.6K 1/8 w 1%
R18,19	991249.9	Res 4.99K 1/8 w 1%
R20	999333	Res 33K 1/4 w 5%
R21	990310	Pot 10K
R22-24	999327	Res 27K 1/4 w 5%
R25	998610	Res 10 Meg 1/2 w 5%
R26	not used	
R27-29	998610	Res 10 Meg 1/2 w 5%
R30,31	999327	Res 27K 1/4 w 5%
R32	991366.5	Res 66.5K 1/8 w 1%
R33	991280.6	Res 8.06K 1/8 w 1%
R34	991310.2	Res 10.2K 1/8 w 1%
R35	999347	Res 47K 1/4 w 5%
R36,37	999420	Res 200K 1/4 w 5%
R38,39	999410	Res 100K 1/4 w 5%
R40	999247	Res 4.7K 1/4 w 5%
R41	999110	Res 100 1/4 w 5%
R42	995005	Res 5, 3 w 5%
R43	not used	
R44	999347	Res 47K 1/4 w 5%
R45	999210	Res 1K 1/4 w 5%
R46,47	999410	Res 100K 1/4 w 5%
R48	991268.1	Res 6.81K 1/8 w 1%
R49	991132.4	Res 324 1/8 w 1%
R50	991090.9	Res 90.9 1/8 w 1%
R51,52	991010	Res 10 1/8 w 1%
R53	991090.9	Res 90.9 1/8 w 1%
R54	991271.5	Res 7.15K 1/8 w 1%
R55	995002.00	Res 2 3 w 1%
R56,57	999410	Res 100K 1/4 w 5%
R58	999310	Res 10K 1/4 w 5%
R59	990010C	Pot Bourns 3339P10
R60	991119.6	Res 196 1/8 w 1%
R61	999410	Res 100K 1/4 w 5%

DESIGNATOR	KRONOS P/N	DESCRIPTION
R62	990210C	Pot 1K
R63	991319.6	Res 19.6K 1/8 w 1%
R64	999568	Res 6.8 Meg 1/4 w 5%
R65	991234	Res 3.4K 1/8 w 1%
R66	999420	Res 200K 1/4 w 5%
R67	990110C	Pot 100
R68	991184.5	Res 845 1/8 w 5%
R69	999168	Res 680 1/4 w 5%
R70	990020C	Pot 20
R71	991073.2	Res 73.2 1/8 w 1%
R72	990310	Pot 10K
R73	999310	Res 10K 1/4 w 5%
R74	999447	Res 470K 1/4 w 5%
R75	990310	Pot 10K
R76,77	999410	Res 100K 1/4 w 5%
R78	999520	Res 2 Meg 1/4 w 5%
R79	999610	Res 10 Meg 1/4 w 5%
R80	999527	Res 2.7 Meg 1/4 w 5%
R81	999320	Res 20K 1/4 w 5%
R82	999268	Res 6.8K 1/4 w 5%
R83	999527	Res 2.7 Meg 1/4 w 5%
C1,2	998110-1K	Disc 100pf KV
C3	985410-80	Polyfilm 0.1 mf 80V
C4	986410-100	Cerm 0.1 mf 100V
C5,6	988410-20	Disc 0.1 mf 20V
C7	985410-80	Polyfilm 0.1 mf 80V
C8	988110-1K	Disc 100 pf 1KV
C9,10	988322-25	Disc .022 mf 25V
C11	985410-80	Polyfilm 0.1 mf 80V
C12	982422-80	Polyfilm 0.22 mf 80V
C13	981510-35	Tant 1 mf 35V
C14	988110-1K	Disc 100 pf 1KV
C15	988210-1K	Disc 100 pf 1 KV
C16	988110-1K	Disc 100 pf 1KV
Q1	965087	Tran 2N 5087
Q2	965400	Tran 2N 5400
Q3	962222	Tran 2N 2222
Q4,5	965087	Tran 2N 5087
Q6	965400	Tran 2N 5400
Q7	962920	Tran 2N 2920
Q8-12	963904	Tran 2N3904
Q13	964410	Tran 2N 4410
Q14	965087	Tran 2N 5087
Q15	962907	Tran 2N 2907
Q16	964036	Tran 2N 4036
Q17	965190	Tran 2N 5190
Q18	965087	Tran 2N 5087
Q19	964410	Tran 2N 4410